Technical Reference

Tektronix

Tektronix Logic Analyzer Family Performance Verification and Adjustment Procedures Version 3.2 Software

070-9776-04

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

www.tektronix.com

Tektronix, Inc., 14200 SW Karl Braun Drive, Beaverton, OR 97077

WARRANTY

Tektronix warrants that the products that it manufactures and sells will be free from defects in materials and workmanship for a period of one (1) year from the date of shipment. If a product proves defective during this warranty period, Tektronix, at its option, either will repair the defective product without charge for parts and labor, or will provide a replacement in exchange for the defective product.

In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

This warranty shall not apply to any defect, failure or damage caused by improper use or improper or inadequate maintenance and care. Tektronix shall not be obligated to furnish service under this warranty a) to repair damage resulting from attempts by personnel other than Tektronix representatives to install, repair or service the product; b) to repair damage resulting from improper use or connection to incompatible equipment; c) to repair any damage or malfunction caused by the use of non-Tektronix supplies; or d) to service a product that has been modified or integrated with other products when the effect of such modification or integration increases the time or difficulty of servicing the product.

THIS WARRANTY IS GIVEN BY TEKTRONIX IN LIEU OF ANY OTHER WARRANTIES, EXPRESS OR IMPLIED. TEKTRONIX AND ITS VENDORS DISCLAIM ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. TEKTRONIX' RESPONSIBILITY TO REPAIR OR REPLACE DEFECTIVE PRODUCTS IS THE SOLE AND EXCLUSIVE REMEDY PROVIDED TO THE CUSTOMER FOR BREACH OF THIS WARRANTY. TEKTRONIX AND ITS VENDORS WILL NOT BE LIABLE FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES IRRESPECTIVE OF WHETHER TEKTRONIX OR THE VENDOR HAS ADVANCE NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Ground the Product. This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

The common terminal is at ground potential. Do not connect the common terminal to elevated voltages.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone

Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power

To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On

Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preventing Electrostatic Discharge

CAUTION. *Static discharge can damage internal semiconductor components. Follow the guidelines listed below to avoid product damage.*

When performing service that requires internal access to an instrument, adhere to the following precautions to avoid damaging internal modules or their components:

- Avoid handling modules or components in areas that have floors or work surfaces capable of generating a static charge.
- Spray carpeted work areas with a solution of equal parts of water and fabric softener.
- Wear clothing made from materials that do not accumulate static charges. Wool (and some artificial fibers) build up static charges readily; cotton conducts electricity and resists static accumulation.
- Minimize the handling of static-sensitive devices.
- Transport and store static-sensitive devices in their protected containers or on a metal rail. Label any package that contains static-sensitive parts.
- Service instruments and modules at grounded static-free work stations.
- Do not allow any device capable of generating a static charge on work station surfaces.
- Wear a grounding wrist strap while working with static-sensitive devices.
- Handle circuit boards by their edges, if possible.
- Do not slide static-sensitive components over any surface.
- Do not use high-velocity compressed air to clean or dry components or modules.

Preface

This manual contains performance verification and adjustment information for the Tektronix Logic Analyzer Family hardware components. Each section covers an individual hardware component such as a mainframe, module, or adjustment fixture and includes the following information:

- An introduction that describes the procedures
- Equipment lists required to perform the procedures
- Functional verification procedures to quickly determine that the component operates properly (as for a brief incoming inspection)
- Certification test procedures and Calibration Data Reports
- Performance verification procedures to ensure the component operates properly and meets warranted specifications
- Adjustment procedures used to adjust the component to meet its warranted specifications

This manual also includes an introduction with important overview information, and an appendix with a parts list and an exploded view of the Logic Analyzer Adjustment and Verification fixture.

Naming Conventions

This manual uses the following abbreviated names for the full product name throughout the text:

Full product name	Abbreviated name
TLA600 Series Logic Analyzer	TLA600
TLA704 or TLA714 Color Portable Mainframe	portable mainframe
TLA711 or TLA720 Color Benchtop Chassis	benchtop chassis
TLA711 or TLA720 Color Benchtop Controller	benchtop controller
TLA7XM Expansion Mainframe	expansion mainframe
TLA7Lx, TLA7Mx, TLA7Nx, TLA7Px, or TLA7Qx Logic Analyzer Module	LA module or LA
TLA7Dx and TLA7Ex Digital Storage Scope	DSO module
TLA7PG2 Pattern Generator Module	pat gen module
Device Under Test / System Under Test	DUT / SUT

Throughout this manual, the term “module” refers to a LA module, a DSO module, an expansion module, or a benchtop controller module.

Service Offerings

Tektronix provides service to cover repair under warranty as well as other services that are designed to meet your specific service needs.

Whether providing warranty repair service or any of the other services listed below, Tektronix service technicians are well equipped to service the Tektronix Logic Analyzer Family products. Tektronix technicians train on Tektronix products; they have access to the latest information on improvements to the products as well as the latest new product upgrades. *Services are provided at Tektronix Service Centers and on-site at your facility, depending on your location.*

Warranty Repair Service

Tektronix technicians provide warranty service at most Tektronix service locations worldwide. The Tektronix product catalog lists all service locations worldwide or you can visit us on our *Customer Services World Center* web site at Tektronix.com/Measurement/Service. See our latest service offerings and contact us by email.

Calibration and Repair Service

In addition to warranty repair, Tektronix Service offers calibration and other services which provide cost-effective solutions to your service needs and quality-standards compliance requirements. Our instruments are supported worldwide by the leading-edge design, manufacturing, and service resources of Tektronix to provide the best possible service.

The following services can be tailored to fit your requirements for calibration and/or repair of the Tektronix Logic Analyzer Family products.

Service Options. Tektronix Service Options can be selected at the time you purchase your instrument. You select these options to provide the services that best meet your service needs. These service options are listed on the *Tektronix Service Options* page at the beginning of this manual.

Service Agreements. If service options are not added to the instrument purchase, then service agreements are available on an annual basis to provide calibration services or post-warranty repair coverage for the Tektronix Logic Analyzer Family products. Service agreements may be customized to meet special turn-around time and/or on-site requirements.

Service on Demand. Tektronix also offers calibration and repair services on a "per-incident" basis that is available with standard prices for many products.

Self Service. Tektronix supports repair to the replaceable-part level by providing for circuit board exchange.

Use this service to reduce down-time for repair by exchanging circuit boards for remanufactured ones. Tektronix ships updated and tested exchange boards. Each board comes with a 90-day service warranty.

For More Information. Contact your local Tektronix service center or sales engineer for more information on any of the Calibration and Repair Services just described.

Contacting Tektronix

Phone	1-800-833-9200*
Address	Tektronix, Inc. Department or name (if known) 14200 SW Karl Braun Drive P.O. Box 500 Beaverton, OR 97077 USA
Web site	www.tektronix.com
Sales support	1-800-833-9200, select option 1*
Service support	1-800-833-9200, select option 2*
Technical support	Email: techsupport@tektronix.com 1-800-833-9200, select option 3* 1-503-627-2400 6:00 a.m. – 5:00 p.m. Pacific time

*** This phone number is toll free in North America. After office hours, please leave a voice mail message.**
Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.

Introduction

Introduction

This manual contains instructions for testing the performance and adjustment of the following instruments:

- TLA600 Series Logic Analyzers
- TLA704 and TLA714 Portable Mainframes
- TLA711 and TLA720 Benchtop Chassis
- TLA711 and TLA720 Benchtop Controllers
- TLA7Lx, TLA7Mx, TLA7Nx, TLA7Px, and TLA7Qx Logic Analyzer Modules
- Logic analyzer probes (tested with the associated logic analyzer)
- Logic Analyzer Module adjustment/verification fixture
- TLA7Dx and TLA7Ex Digitizing Oscilloscope Module
- TLA7PG2 Pattern Generator Modules
- Pattern generator probes (tested with the associated pattern generator module)

Four levels of testing are provided:

- Functional verification procedures
- Performance verification procedures
- Certification test procedures and Calibration Data Reports
- Adjustment procedures

Not all of the components of the Tektronix Logic Analyzer Family require all four levels of testing. Table 1–1 on page 1–2 lists the components of the logic analyzer family and the levels of testing described in this manual.

Certain instruments, such as the Termination Board (used with pattern generator modules), do not require any testing or certification.

Table 1–2 lists the typical order of procedures needed for verifying the performance and adjustment of the instruments. These procedures assume that you are familiar with operating the instruments.

Table 1–1: Levels of testing and adjustment

Component/product	Functional verification	Certification	Performance verification	Adjustment
TLA600 Series Logic Analyzers	Yes	Yes	Yes	Yes, software controlled
TLA714 and TLA714 Portable Mainframes	Yes	Yes	Yes	No
TLA711 and TLA720 Benchtop Chassis	Yes	No	Yes	No
TLA711 and TLA720 Benchtop Controllers	Yes	Yes	Yes	No
Logic analyzer modules (all versions)	Yes	Yes, software controlled	Yes, software controlled	Yes, software controlled
Logic Analyzer Adjustment and Verification fixture	Yes	Yes	Yes	Yes
TLA7Dx/TLA7Ex Digitizing Oscilloscope Module	Yes	Yes, software controlled	Yes, software controlled	Yes, software controlled
TLA7PG2 Pattern Generator modules	Yes	No	Yes	No

Table 1–2: Typical order of procedures

Instrument type	Annual performance verification, calibration, re-certification[1]	Adjustment, performance verification, calibration, re-certification[1] following board repair
Mainframes and benchtop controller	Run performance verification procedure	Run performance verification procedure
TLA600 Logic Analyzers and all LA modules	1. Run performance verification procedure 2. If module fails performance verification procedure, then run the adjustment procedure 3. Rerun performance verification if step 2 is done	1. Run adjustment procedure 2. Run performance verification procedure
Logic Analyzer Adjustment and Verification fixture	Run performance verification procedure[2]	Run performance verification procedure
Pattern Generator Modules	Run the functional verification and the performance verification procedures	Run the functional verification and the performance verification procedures
DSO modules	1. Run performance verification procedure 2. If module fails performance verification procedure, then run the adjustment procedure 3. Rerun performance verification if step 2 is done	1. Run performance verification procedure 2. If module fails performance verification procedure, then run the adjustment procedure 3. Rerun performance verification if step 2 is done

1 **Refer to the appropriate certification sections in this document for all certification procedures**

2 **The Logic Analyzer Adjustment and Verification fixture requires calibration every two years**

Functional Verification Procedures

Functional verification procedures verify the basic functionality of the instrument inputs, outputs, and basic instrument actions. These procedures include power-on and extended diagnostics, self calibration, as well as semi-automated or manual check procedures. These procedures can be used for incoming inspection purposes.

Certification Test Procedures

Certification procedures are used to certify the accuracy of an instrument and provide a traceability path to national standards. Certification data is recorded on Calibration Data Reports provided with this manual. Calibration Data Reports are produced for the TLA600 Logic Analyzers, LA modules, and DSO modules as an output from the PV/Adjust software.

Performance Verification Procedures

Performance verification procedures confirm that a product meets or exceeds the performance requirements for the published specifications documented in the *Tektronix Logic Analyzer Family User Manual*. Refer to Figure 1–1 on page 1–4 for a graphic overview of the procedures.

Adjustment Procedures

Adjustment procedures check for and, if necessary, correct any adjustment errors discovered when performing functional or performance verification procedures. The adjustment procedures documented in this manual are controlled by software, except for the procedures for the adjustment/verification fixture.

Some procedures require user intervention to move probes or change test equipment settings. The adjustment software is part of the self-calibration routines in the logic analyzer application software and the PV/Adjust software provided with the CD that accompanies this manual.

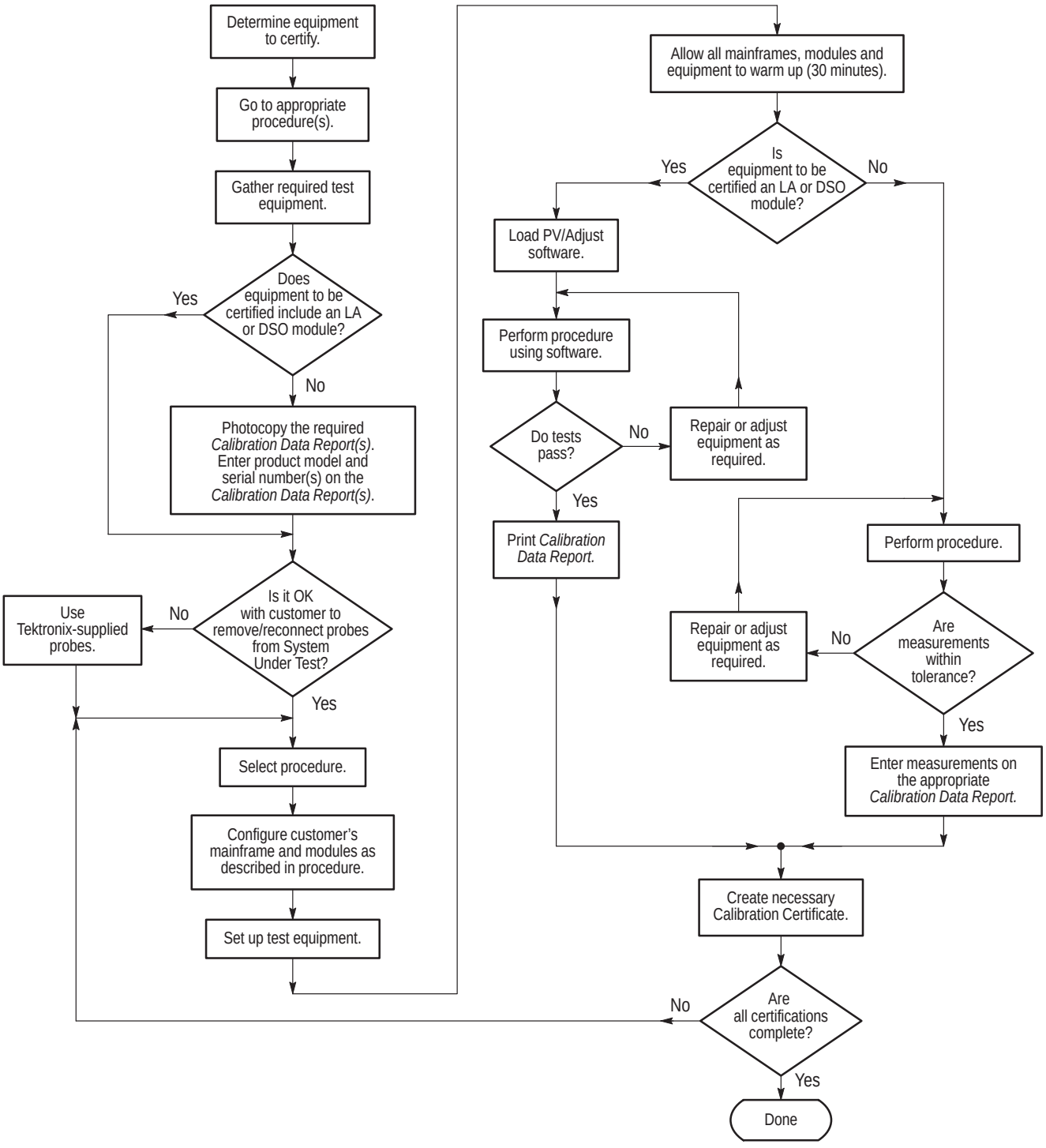


Figure 1–1: Calibration/certification procedure flow chart

Test Equipment

The procedures in this manual use external, traceable signal sources to directly test characteristics that are designated as checked (✓) in the *Specifications* section of the *TLA 700 Series Logic Analyzer User Manual*. Table 1–3 shows the required equipment list. Always warm up the equipment for 30 minutes before beginning the procedures.

Table 1–3: Test equipment

Item number and description	Minimum requirements	Example	Where used
1. Mainframe	TLA700 Series Mainframe	Benchtop Chassis or Portable Mainframe	All procedures, except TLA600 procedures
2. Controller	TLA700 Series Controller	Benchtop Controller used with the Benchtop Chassis or the embedded controller in the Portable Mainframe	All procedures, except TLA600 procedures
3. TLA700 Series Logic Analyzer Performance Verification & Adjustment Software	On the accompanying CD-ROM	Tektronix part number 063-2856-03	All procedures for the TLA600 Logic Analyzers, LA modules and DSO modules. Includes pat gen module setups
4. Adjustment/verification fixture, with one of the following Power Supplies: USA/CAN Europe Japan United Kingdom	 12 V, 1.5 A 12 V, 1.5 A 12 V, 1.5 A 12 V, 1.5 A	Tektronix part number 671-3599-XX Tektronix part numbers: 119-4855-XX 119-4856-XX 119-4859-XX 119-4857-XX	Most procedures for the LA module
5. DSO probe calibration fixture	One required	Tektronix part number 671-3930-XX	DSO functional verification procedure
6. Oscilloscope	1 GHz bandwidth Delay time accuracy ±25 ppm over any ≥ 1 ms interval	Tektronix TDS 784D	Adjustment/verification fixture procedures and pattern generator procedures
7. DSO probes	Three required, with < one-inch ground leads	Tektronix P6243 or P6245 probe, with std. accessories	Most procedures for the DSO and Pattern Generator modules
8. Logic analyzer probes	Two required	Tektronix P6417 or P6418 Logic Analyzer probes	Most procedures for TLA600 and the LA module
9. High density logic analyzer probe (optional)	One required	Tektronix P6434 Logic Analyzer probe	Most procedures for TLA600 and the LA module
10. Pattern Generator module	One required	TLA7PG2	Merge and Deskew pattern generator procedures
11. Pattern Generator probe cable	Eight required	Tektronix part number 012-A212-00	Pattern generator procedures

Table 1–3: Test equipment (Cont.)

Item number and description	Minimum requirements	Example	Where used
12. TTL/CMOS Pattern Generator probes	Four required	Tektronix P6470 Pattern Generator probes	Most pattern generator procedures
13. ECL Pattern Generator probes	Four required	Tektronix P6471 Pattern Generator probes	Most pattern generator procedures
14. Termination board	Two required	Tektronix part number 067-A016-00	Most pattern generator procedures
15. Frequency counter	Frequency accuracy: <0.0025% Frequency range: 1 kHz to 100 MHz	Hewlett Packard 5314A	Portable Mainframe and Benchtop Controller procedures
16. Function generator	Amplitude: 4V Offset: 2 V (50 Ω termination) Frequency: 1 MHz or higher	Tektronix AFG2020	Pattern generator procedures
17. Power supply	Voltage: –2 V Current: 1 A	METRONIX 524B	Pattern generator procedures
18. BNC Cable	Impedance: 50 Ω, Length: 24 in (two required)	Tektronix part number 012-1342-XX	Pattern generator procedures
19. T-Connector	One required	Tektronix part number 103-0030-XX	Pattern generator procedures
20. SMB-to-BNC cable	One required	Tektronix P6041	PV procedures for the Benchtop Controller
21. Adapter, male BNC-to-male BNC	One required	Tektronix part number 103-0029-XX	DSO procedures
22. Miniature probe-to-square pin adapters	Two required	Tektronix part number 103-0177-XX	Portable Mainframe (power supply check)
23. 0.025-inch square pin	3/4-inch length, (two required)	Tektronix part number 131-1426-XX	Portable Mainframe (power supply check)
24. Digital multimeter with test leads	DCV accuracy: 0.1% from –10 V to +100 V	Tektronix DMM 900 Series	All procedures except Benchtop Controller
25. Connector, dual-banana	Female BNC-to-dual banana	Tektronix part number 103-0090-XX	PV procedures for the LA and DSO module
26. Voltage reference	Accuracy: ≤0.01%	Data Precision 8200	PV procedures for the LA and DSO module
27. Capacitor[1]	0.1 μF, 200 V	Tektronix part number 283-0189-XX	PV procedures for the LA and DSO module
28. Cable, dual-input	Female BNC-to-dual male BNC	Tektronix part number 067-0525-XX	PV procedures for the DSO module
29. Adapter, N-to-BNC	Male type N-to-female BNC	Tektronix part number 103-0045-XX	PV procedures for the DSO module
30. Adapter, SMA-to-BNC	Female type SMA-to-female BNC	Tektronix part number 015-1018-XX	DSO procedures

Table 1–3: Test equipment (Cont.)

Item number and description	Minimum requirements	Example	Where used
31. Cable, precision 50 Ω coaxial	50 Ω, 36 in, male-to-male BNC connectors	Tektronix part number 012-0482-XX	All procedures except Benchtop Chassis
32. Generator, function	Frequency range: 1 Hz to 20 MHz Frequency accuracy: 0.1% Amplitude range: 10 mV to 20 V_{p-p}	Hewlett Packard 3325B	PV procedures for the DSO module
33. Generator, sine wave	Frequency range: 100 kHz to 1005 MHz Frequency accuracy: <6 ppm Amplitude: 2 mV to 1.5 V_{RMS} Accuracy: <0.35 dB	Gigatronics 6061	PV procedures for the DSO and LA module
34. Power meter with sensor	Bandwidth: >1.2 GHz Accuracy: 0.2 dB Sensitivity: 500 pW to 20 mW	Rohde & Schwarz NRVS with model NRV-Z4 Sensor	DSO adjustment procedure #4
35. Adapter, N-to-BNC (used only with power meter)	Female type N-to-male BNC	Tektronix part number 103-0058-XX	DSO adjustment procedure #4
36. 50 Ω power divider (used only with power meter)	Provide load isolation between equipment Maximum VSWR: 1.50	Tektronix part number 015-0565-XX	DSO adjustment procedure #4
37. SMA-to-BNC adapters (used only with power meter)	For use with the 50 Ω power divider (three required)	Tektronix part number 015-1018-XX	DSO adjustment procedure #4
38. Printer with cable (optional, used to print Calibration Data Reports)	PC-compatible, continuous feed, prints ASCII text, connects to EPP connector	Any general purpose printer	Printing test results for the LA and DSO module

1 **The capacitor is installed across the Data Precision 8200 output terminals to reduce noise. If your voltage reference produces <4 mVp-p of noise, external noise reduction is not necessary.**

Software Installation and Removal Instructions

These procedures describe loading and unloading the PV/Adjust software. It is recommended you have ≥ 10 MB of free space on the hard drive before installing the software.

NOTE. *The Performance Verification software is located on the CD accompanying this manual. If you have a TLA704 Portable Mainframe or TLA711 Benchtop Mainframe, you must connect an external PCMCIA CD-ROM drive to load the software. Contact your local Tektronix representative for information on ordering and external PCMCIA CD-ROM drive.*

NOTE. *This installation program uses parameters you supply to create a custom start-up file in your hard disk directory.*

The batch file enables the software to configure your instrument properly before it runs the program.

1. Power on the instrument.
2. Exit the Application.

Verify PV/Adjust Software Version

If your logic analyzer already has PV/Adjust software loaded on it, you must verify that the version is the same as the version printed on the CD that accompanies this manual.

If the version of the PV/Adjust software loaded on your logic analyzer is an earlier version, you must delete the earlier version.

Verify Directories

If your logic analyzer already has a directory named Tekcats or Temptek on the hard drive, the software installation cannot be completed. Follow these instructions to verify the directory is not present:

1. Select Start → Programs → Windows Explorer.
2. From the Exploring window select Tools → Find → Files or Folders.
3. Select the Name & Location tab, and search for the following directories:
   - Tekcats
   - Temptek
4. If either directory is found follow the instructions under *Removing the Software* beginning on page 1–10 to remove the software and the directories.

Install the PV/Adjust Software

Follow these instructions to install the PV/Adjust software and the pattern generator setup files.

1. Close all open windows on the desktop.
2. Insert the Performance Verification & Adjustment Software CD in the CD-ROM drive.
3. Click the My Computer Icon and double-click the CD-ROM drive.
4. Double-click the TLA Windows 98PV folder on the CD.
5. Double-click the Disk1 folder.
6. Double-click the Setup.exe icon to begin the installation program.
7. Follow the on-screen instructions to install the software on the hard disk.
8. After the installation is complete, go back to the top-level folder on the CD and double-click on the Pattern Generator folder.
9. Double-click the Disk1 folder.
10. Double-click the Setup.exe icon to begin the installation program.
11. Follow the on-screen instructions to install the pattern generator setup files on the hard disk.

Install the Font

The required Lucida Console (True Type) fonts are resident in Windows. To confirm that the Lucida font has been installed follow these directions:

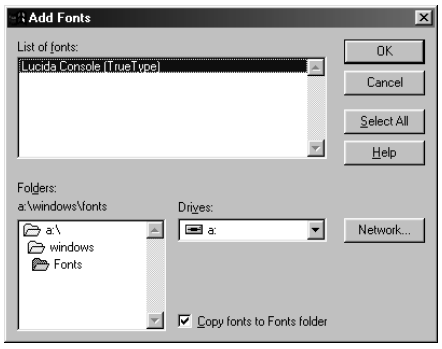
1. Select Start → Settings → Control Panel.
2. Double-click the Fonts icon.
3. Verify that the Lucida Console (True Type) font icon is present, as shown in Figure 1–2.

Figure 1–2: Lucida Console font icon

If the Lucida Console (True Type) font is not installed, complete the following steps:

1. If you haven not already done so, insert the Performance Verification & Adjustment Software CD in the CD-ROM Drive.

2. Select Start → Settings → Control Panel.
3. Double-click the Fonts icon.
4. In the Fonts window, go to the File menu and select Install New Font...
5. In the Add Fonts dialog box under Drives, select the CD-ROM drive.
6. Under the Folders list, double-click on the Fonts folder.
7. Select Lucida Console (True Type) as shown below.



8. Click the OK button. The new font will be added to the Fonts folder.
9. Close the all open windows.
10. Remove the CD from the CD-ROM drive.

This completes the software installation procedure.

Removing the Software

Use the following procedure to remove the PV/Adjust software from the instrument. These steps are necessary when you want to upgrade the PV software.

1. Select Start → Programs → Windows Explorer.
2. Using Windows Explorer, click the C:\ Tekcats folder.
3. Go to the File menu and select Delete to delete the folder.
4. Repeat steps 1 through 3 to delete the Temptek folder if it exists.
5. Select Start → Settings → Taskbar & Start Menu.
6. Click the Start Menu Programs tab.
7. Click the Remove button and then select TLA Performance Verification from the list.

8. Click the Remove button again to remove the selection from the Start menu.
9. Select Start → Settings → Control Panel → Fonts.
10. Select the Lucida Console font.
11. Select Delete from the File menu to remove the font.

Using the Software

The PV/Adjust software is required to complete the performance verification, adjustment and calibration/certification procedures for the TLA600 Logic Analyzers, the LA modules, and for the DSO modules. A separate series of program files are required for the pattern generator modules. Software is not required to perform any checks on the mainframes or any other subcomponents.

Pattern Generator Setup Files

The PV/Adjust software used to verify the pattern generator modules consists of setup files rather than executable software. To use the pattern generator setup files complete the following steps:

1. Verify that your module configuration matches the setup as called for in the writtern procedure (for some of the setups you will need to merge or unmerge modules).
2. Select Load Module from the File menu; the Load Module dialog box appears.
3. Click the Browse button and navigate to the C:\Program Files\Tektronix Pattern Generator\PV folder.
4. Double-click on the file name; the Load Module dialog box reappears with the file name and module name under the Module list.
5. Click OK to load the module setup. A dialog box may appear reminding you that the current module settings and data will be lost.
6. Click Yes to confirm your choice.
7. Follow the remaining written procedures.

LA and DSO Performance Verification and Adjustment Software

The logic analyzer and DSO software consists of executable software files. Use the software in conjunction with this manual to set up and perform the adjustment procedures or the performance verification procedures. Use this manual in the following manner:

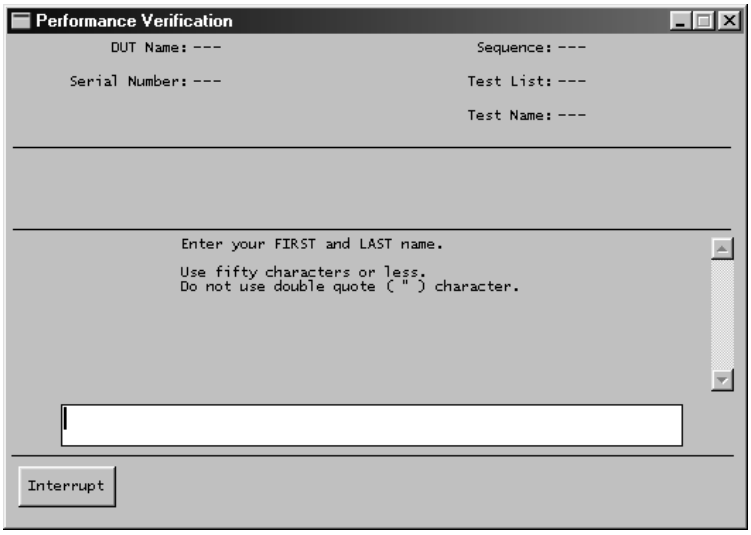
- To provide an overview of each test
- To identify the prerequisites for each test
- To identify the required test equipment
- To connect the external test equipment for each test

Running the LA and DSO Software

Use the following steps to start and run the logic analyzer and DSO software:

1. Allow the instruments to warm up for at least 30 minutes before beginning the procedure.
2. Quit all applications including the TLA application.
3. Select Start → Programs → TLA Performance Verification.
4. To run the PV/Adjust software, select one of the following:
   - For the TLA7Dx and TLA7Ex DSO modules, select DSO PV.
   - For the TLA700 logic analyzer modules, select LA 7XX PV.
   - For the TLA600 Logic Analyzer, select LA 6XX PV.

5. Follow the instructions on the screen to enter the name you want to appear in the User Name field as shown below. This name will appear on the Calibration Data Reports.



6. Click Enter to continue.

7. The program lists several different modules, referred to as DUT (Device Under Test). Enter the number corresponding to the module type that you want to test; then click Enter to continue.

   The screen will display an error message if the DUT chosen does not match the installed DUT.

8. Enter the complete serial number of the DUT (for example, B010100). Click Enter to continue.

9. Verify the serial number entry; then click Enter to continue.

   If you select no, a prompt asks you to enter the serial number again.

10. The program lists sequences for PV (performance verification) and ADJ (adjustments). Enter a number to select which sequence you want and click Enter to continue.

11. If an instrument is being tested, the program lists the different probe types available for testing. Enter the appropriate number corresponding to your probe and then click Enter to continue.

12. Enter the operating temperature in degrees C (entries in the range of 20 to 30 degrees are valid). Click Enter to continue.

13. Enter the operating humidity as a percentage (0% to 100% entries are valid). Click Enter to continue.

14. Determine which sequence to run:

    - RUN FULL SEQUENCE runs the entire sequence from beginning to end. This is the recommended selection.
    - RUN PARTIAL SEQUENCE runs part of the full sequence. The sequence runs from the selected starting point to the end of the sequence.
    - SELECT TEST(S) runs only the selected tests. To run a single test, enter the test number. To run multiple tests, enter a comma-separated list of numbers or a hyphen-separated list of numbers.

    Enter the number next to your choice and click Enter to continue.

15. Follow the on-screen instructions to connect and adjust test equipment. You can also refer to the connection diagrams provided in this manual for each test.

16. When testing is completed, disconnect the test equipment.

Troubleshooting

If the test you are attempting to run fails, do the following:

- Check the settings and connections of the test equipment used in the procedure.
- If you are using the adjustment/verification fixture, verify that the LED is lighted and that the jumper positions and external connections are correct.
- Rerun mainframe or module diagnostics and module self-cal, then rerun the test(s) which failed.

If the test(s) still do not pass, the mainframe or module might need further troubleshooting.

Using the Interrupt Button

While the program is running, you can interrupt the program to rerun a test, start over, or to exit the program by clicking the Interrupt button (shown below).

The program will then provide a list of choices. Enter the number next to the choice that you want and click Enter.

***NOTE**. If you interrupt a test before it has completed, you must restart the test to obtain valid test data.*

Some tests such as Internal Cal do not allow interrupts. If you stop these tests using more aggressive methods, you may have to reboot the instrument.

Obtaining Test Results

The results of all tests can be stored in a file on the hard disk. You can view the test results, print the test results to a printer, or save the test results in another file on the hard disk.

After running the performance verification procedures, you should create a calibration data report for certification purposes. Refer to *Calibration Data Reports* for details on using the resultant test data with the Calibration Data Report.

Calibration Data Reports

The Calibration Data Reports in this manual are intended to be copied and used for calibration/certification procedures. Some of the certification procedures require you to record data from manual measurements on the Calibration Data Reports directly. The TLA600 Logic Analyzer, the LA module, and the DSO module procedures require that you obtain the test results from the file created by the PV/Adjust software.

After completing the performance verification procedures or the certification procedures, you can fill out a Calibration Data Report to keep on file with your instrument. Calibration Data Reports are provided at the end of the certification procedures in each chapter of this manual, except for the TLA600 Logic Analyzer, the LA module, and DSO module. Calibration Data Reports for these instruments are generated by the PV/Adjust software. The Calibration Data Reports list those product attributes and specifications upon which product accuracy depends.

Retrieving Test Data from the PV/Adjust Software

The program stores the test results in a file containing the module name and serial number (for example, TLA7E2.B020123). The file is located under the following path: C:\Tekcats\Rpt.

***NOTE**. If you want to save the content of the Report file, you must rename or copy the Report file using the Windows file utilities such as Explorer.*

The Report file will be overwritten the next time you run the PV/Adjust software and print or view a new set of test data.

After completing a full or partial test sequence (or just before you exit the program) you can generate the test data and write it to a file. You have the option of printing the file, viewing the file on screen, or transferring the file to another directory or host computer.

You can print the test data directly from the program. Ensure that a printer is connected to your logic analyzer and follow the on-screen instructions to print the test results.

If a printer is not available, you can view the test results directly from the screen, or you can copy the test results to a different file or folder/host computer for future use.

Field Adjust/PV Software Housekeeping

The PV/Adjust software creates data log files (.dlf files) that store program data. The .dlf files are used by the PV/Adjust software to generate the view data and print out options. Each .dlf file is identified by the product serial number; for example, B010100.dlf. The files are stored in the Tekcats folder under each TLA7xx folder. To conserve disk space, you must occasionally delete the .dlf files.

TLA600 Series Logic Analyzer

TLA600 Series Logic Analyzer Functional Verification

This section contains instructions for performing the functional verification procedure. This procedure provides an easy way to check the basic functionality of the TLA600 Series Logic Analyzer.

Tests Performed

Table 2–1 lists the functional verification procedures that are available for the TLA600 Logic Analyzer and probes.

Table 2–1: TLA600 Functional verification procedures

Instrument	Procedure	Adjustment/verification fixture required
Logic Analyzer	Power-up diagnostics	No
Logic Analyzer	Extended diagnostics	No
Logic Analyzer	Mainframe diagnostics	No
Logic Analyzer	QA+Win32 diagnostics	No
P6417, P6418, or P6434 logic analyzer probes	Signal Input check	Yes

NOTE. *Running the extended diagnostics will invalidate any acquired data. If you want to save any of the acquired data, do so before running the extended diagnostics.*

If any check within this section fails, refer to the *TLA600 Series Logic Analyzer Service Manual* for corrective action.

The functional verification procedure consists of the following parts:

- Module self tests and power-on diagnostics
- Probe verification

This procedure provides a functional check only. If more detailed testing is required, perform the *Performance Verification Procedure* after completing this procedure.

Test Procedure

You will need a TLA600 Series Logic Analyzer to complete this test procedure.

Equipment required	Cable, 50 Ω coaxial (item 31)
Prerequisites	Warm-up time: 30 minutes

Perform the following tests to complete the functional verification procedure.

Extended Diagnostics

Do the following steps to run the extended diagnostics:

NOTE. *Perform the following steps to complete the functional verification procedures. Before beginning this procedure, be sure that no active signals are applied to the logic analyzer. Certain diagnostic tests will fail if signals are applied to the probe during the test.*

1. Power on the instrument and wait for the system application to start.
2. Go to the System menu and select Calibration and Diagnostics.
3. Verify that all power-on diagnostics pass.
4. Click the Extended Diagnostics tab.
5. Select All Modules, All Tests (top line) and click the Run button on the property sheet.

   The diagnostics software performs each one of the tests listed in the menu under the module selection. All tests that displayed an Unknown status will change to a Pass or Fail status depending on the outcome of the tests.
6. Scroll through the test results for the instrument and verify that all tests pass.

NOTE. *If Extended Diagnostics fail, run Self Cal for the logic analyzer and then rerun Extended Diagnostics.*

Mainframe Diagnostics

The TLA Mainframe Diagnostics check the functionality of the instrument. To run these diagnostics, do the following steps:

1. Turn off all other applications.
2. Click the Windows Start button.
3. Select Programs from the Start menu.
4. Select Tektronix Logic Analyzer from the Programs menu.
5. Select Tektronix TLA Mainframe Diagnostics from the Tektronix Logic Analyzer menu.
6. Run the mainframe diagnostics. Connect the BNC cable when requested.

When the TLA Mainframe Diagnostics are run, a Mainframe Diagnostics Warning dialog box appears. Clicking OK will initiate a SYSRESET, which will invalidate any acquired data.

QA+Win32

QA+Win32 is a comprehensive software application used to check and verify the operation of the PC hardware in the instrument. To run QA+Win32, you must have either a working keyboard or a working mouse or other pointing device and have Windows running.

CAUTION. *Before running the QA+Win32 tests, check the release notes for possible problems and workarounds.*

To run QA+Win32, follow these instructions:

1. Turn off all other applications.
2. Click the Windows Start button.
3. Select Programs.
4. Select QA+Win32.
5. Run the QA+Win32 diagnostics.

Checking the Cooling Fan Operation

Power on the instrument and inspect the side of the instrument to verify that all six cooling fans are rotating.

Logic Analyzer Probe Functional Verification Procedure

The following procedure checks the basic operation of the probes by verifying that the probes recognize signal activity at the probe tips.

Equipment required	Adjustment/verification fixture (item 4)
Prerequisites	Warm-up time: 30 minutes for instrument and test equipment P6417, P6418, or P6434 probe connected to the instrument[1] Test equipment connected as shown in Figure 2–1 Power-up diagnostics pass SELF_CAL passes

1 **Do not mix probes; only one type of probe can be functionally verified at a time.**

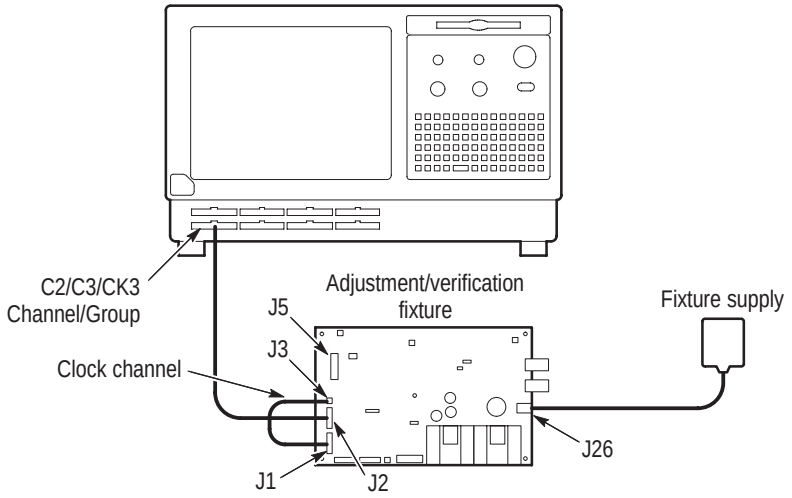


Figure 2–1: Probe functional verification test setup

Test Procedure

Perform the following steps to complete the probe functional verification procedure:

1. Ensure that the jumper at J15 on the adjustment/verification fixture is in the INT position to select the internal 50.065 MHz clock.
2. Open the Setup window and click the Set Thresholds button to display the Probe Threshold dialog box.
3. Adjust the threshold level to 700 mV for all channels.

***NOTE**. These procedures assume a P6418 or P6417 probe is used.*

If you are use a P6434 probe, use J5, the Data Out connector on the adjustment/ verification fixture to verify probe functionality. Observe proper polarity: pin 1 to pin 1.

4. Refer to Figure 2–1 and connect the podlets of the acquisition probe to J1 and J2 on the fixture. Ensure that you connect the ground side of the podlets to the ground side of the connectors.
5. Connect the single clock (CK n) or the qualifier (Q n) channel to one of the J3 CLK OUT connector pairs on the fixture.
6. Return to the Setup window and click the Show Activity button to display the Activity Monitor.
7. Verify that the Activity Monitor shows activity on all probe channels connected to the test fixture.

   Figure 2–2 shows an example of the Activity Monitor. Note the signal activity for clock CK3 and data channels for the C3(7-0) and C2(7-0) groups. Also note that there is no activity on the other groups because the probe podlets are not connected to a signal source (the channels are all high).

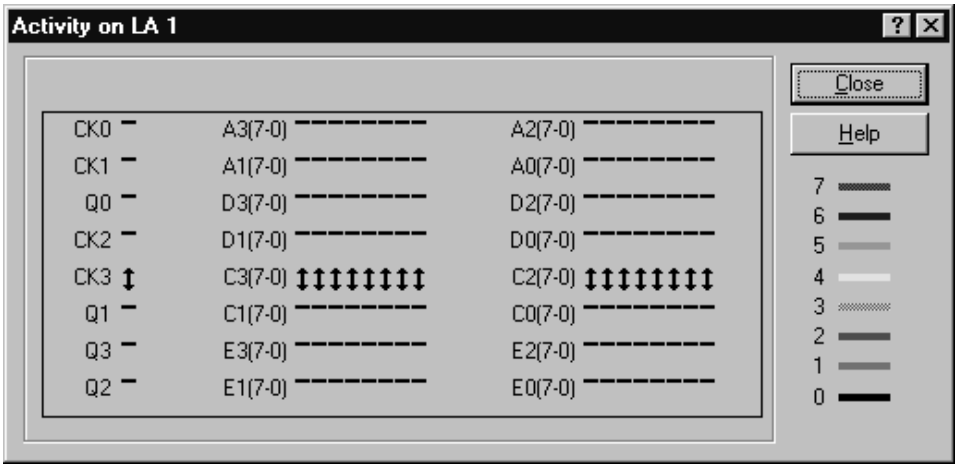


Figure 2–2: Activity Monitor

8. Verify that none of the connected channels are stuck high or stuck low.
9. Disconnect the probe from the fixture and the instrument.
10. Repeat the steps for any remaining probes.
11. Close the Activity Monitor.
12. Return the threshold levels to their former values in the Probe Threshold dialog box.
13. This completes the probe functional verification procedure.

TLA600 Series Certification

Using the performance verification procedures, check the accuracy of the system clock and perform the DC Threshold test. The instrument is certifiable if these parameters meet specifications. Other specifications can also be verified by running the complete performance verification procedures.

Calibration Data Report

TLA600 Logic Analyzer

Instrument model number: _____

Serial number: _____ Certificate number: _____

Verification performed by: _____ Verification date: _____

System Clock Test Data

Characteristic	Specification	Tolerance	Procedure reference	Incoming data	Outgoing data
Clock frequency	10 MHz	±1 kHz (9.9990 MHz-10.0010 MHz)	Page 2–13, Step 5		

Tektronix

TLA600 Series Logic Analyzer Performance Verification

This section contains procedures to verify that the TLA600 series instruments perform as warranted. Verify instrument performance whenever the accuracy or function of your instrument is in question, or as part of an annual calibration/certification.

As a general rule, these tests only need to be done once a year.

Prerequisites

These procedures ask for the serial number of the TLA600 series instrument under test. The serial number and state speed to the instrument is noted on a label on the right side of the back panel.

The tests in this section comprise an extensive, valid confirmation of performance and functionality when the following requirements are met:

- The Tektronix Logic Analyzer application must not be running.
- The PV/Adjust software must be loaded. Refer to *Software Installation and Removal Instructions* on page 1–8.
- The logic analyzer, must have been operating for a warm-up period of at least 30 minutes, and must be operating at an ambient temperature between +20° C and +30° C.
- The logic analyzer must have been last adjusted at an ambient temperature between +20° C and +30° C.
- The logic analyzer must be in an operating environment within the limits described in the *Specifications* section of the *Tektronix Logic Analyzer Family User Manual.*

Tests Performed

The PV/Adjust software contains the tests shown in Table 2–2. Each test verifies one or more parameters. All of the tests check characteristics that are designated as checked (✓) in the *Specifications* section of the *Tektronix Logic Analyzer Family User Manual.*

By running a full PV sequence, you will verify the performance of the logic analyzer.

Table 2–2: TLA600 PV/Adjust software performance verification tests

Performance verification test name	Specification tested
1. System clock (CLK10)[1]	Signal output check
2. FPV_DC_THRESHOLD[1]	Threshold accuracy
3. FPV_SETUP_0F	Setup time
4 FPV_HOLD_0F	Hold time
5. FPV_MAXSYNC	Maximum synchronous clock rate

1 **Certifiable parameter**

Table 2–3 lists the additional characteristics that are designated as checked (✓) in the *Specifications* section of the *Tektronix Logic Analyzer Family User Manual*.

These characteristics are indirectly tested by the PV/Adjust software tests named in the table.

Table 2–3: TLA600 characteristics indirectly checked by the PV/Adjust software performance verification tests

Performance verification test name	Specification tested
1. FPV_SETUP_0F	Minimum recognizable word[1,2]
2 FPV_HOLD_0F	Minimum recognizable word[1,2]
3. All tests	Trigger state sequence rate
4. All tests, and Extended Diagnostics	Internal sampling period[3]

1 **When the setup and hold time tests are both performed, the setup and hold window size is indirectly verified.**

2 **When the setup and hold time tests are both performed, the channel-to-channel skew is indirectly verified.**

3 **When all of the tests are performed, including Extended Diagnostics, the internal sampling period is indirectly verified.**

The procedures in this document assume that you will run a full sequence of tests. Each test includes a simple illustration of the test equipment setups.

Test Equipment

These procedures use external, traceable signal sources to directly test the characteristics that are designated as checked (✓) in the *Specifications* section of the *Tektronix Logic Analyzer Family User Manual.*

In addition to the basic system setup, you will need some of the equipment shown in Table 1–3 on page 1–5 in the *Introduction* section to complete the performance verification procedures. A condensed list of test equipment is provided at the beginning of each test.

Test Procedures

Use the following steps to complete the performance verification procedure. Each procedure includes a table that calls out the equipment used; use Table 1–3 beginning on page 1–5 for equipment specifications. If you substitute equipment, always choose instruments that meet or exceed the minimum requirements specified.

Do the following to check the accuracy of the 10 MHz system clock.

Equipment required	Frequency counter (item 15) Precision BNC cable (item 31)
Prerequisites	Warm-up time: 30 minutes for the logic analyzer and test equipment Power-on, Mainframe, and QA+WIN32 diagnostics pass

1. Connect the frequency counter to the External Signal Out TTL BNC connector on the back of the instrument.
2. Verify that the Tektronix Logic Analyzer application is running.
3. Go to the System window and select System Configuration from the System menu.
4. In the System Configuration dialog box, select 10 MHz Clock from the list of routable signals in the External Signal Out selection box and click OK.
5. Verify that the output frequency at the External Signal Out TTL connector is 10 MHz ±1 kHz. Record the measurement on the Calibration Data Report.
6. In the system configuration dialog box, reset the External Signal Out signal to None.
7. Disconnect the frequency counter.

Using the Software

This section provides a brief overview on using the PV/Adjust software.

NOTE. *If you are testing an instrument that has been repaired, you must complete the adjustment procedures before running the performance verification.*

When using the PV/Adjust software, you will connect external test equipment to the probe inputs in response to prompts on the screen. You will connect the test signals and then instruct the program to continue. The PV/Adjust software automatically selects the LA settings and determines the results of each test.

The results of the tests are recorded in a temporary file and are available upon test completion for completing test records for certification. To obtain partial test information you can also run individual tests or selected groups.

NOTE. *The SELF_CAL test must run successfully before the other tests are performed. The remaining tests can then be performed in any order.*

The PV/Adjust software contains online instructions for performing the performance verification procedure. The basic steps for completing the procedures follow:

1. Start the program, enter user and product identification information.
2. Select either PV or Adj.
3. Select temperature and humidity.
4. Select the probes.

NOTE. *If you are using P6417 or P6418 probes, label one probe as the Reference Probe, and the other probe as the Probe Under Test.*

If you are using a P6434 probe, label the probe channel group identified as the pin 38 side as Probe A. Label the probe channel group identified as the pin 1 side as Probe B; refer to Figure 2–3.

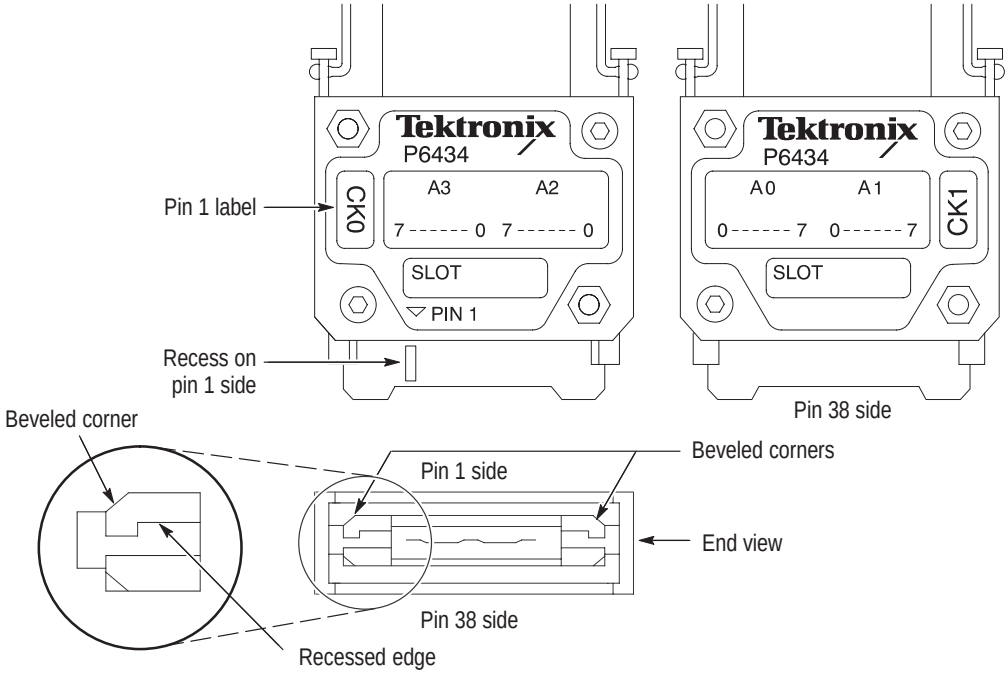


Figure 2–3: P6434 probe detail

5. Select a full test sequence.
6. Connect the test equipment.
7. Set up the test equipment for the output signals described by on-screen instructions and by the connection illustration for each test.
8. Run each test as instructed.

NOTE. *Some tests prompt you for input on whether to "1:Do Section or 2:Skip Section." It is recommended that you select "Do Section" unless you use the software for troubleshooting.*

9. After completing all the tests, view the test results and print them out if performing a certification. Refer to *Retrieving Test Data from the PV/Adjust Software* on page 1–15 for instructions on obtaining test data.

Troubleshooting

If any tests fail, use the following steps to troubleshoot problems:

1. Check all test equipment for improper or loose connections.
2. Check that all test equipment is powered on and has the proper warm-up time.
3. If you are using the adjustment/verification fixture, verify the LED is lighted, jumper positions match the on-screen instructions, and the external connections are correct. (See Figure 2–4 for jumper locations.)
4. Rerun all diagnostics and adjustment procedures.
5. Run the tests a second time to verify the failure.
6. If tests continue to fail, refer to the *TLA600 Series Logic Analyzer Service Manual* for corrective action.

Performance Verification Tests

Use the following tables and figures to set up and execute each procedure.

NOTE. *The illustrations in the following procedures assume that you are using the P6418 or P6417 probes.*

If you have a P6434 probe, use J14 on the adjustment/verification fixture for the DC Threshold test; all other procedures using the P6434 probe use J5, the Data Out connector.

When using either type of probe, always observe correct polarity (GND to GND, pin 1 to pin 1).

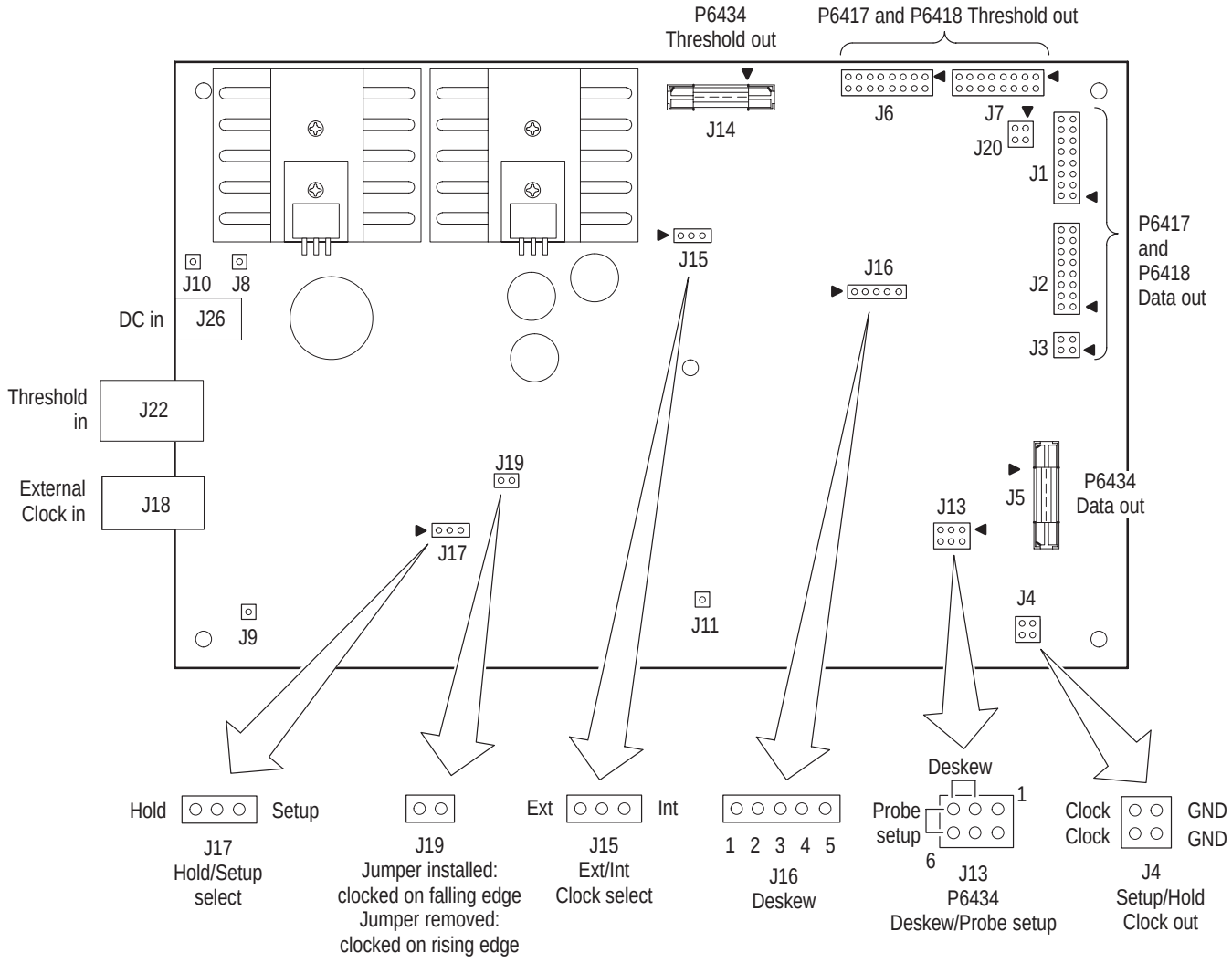


Figure 2–4: Adjustment/verification fixture connections and jumper locations

TLA600 Procedure 1: FPV_DC_Threshold

This procedure verifies the DC Threshold Accuracy of the logic analyzer. This test is performed once and applies to all channels of the instrument.

SW test name	FPV_DC_Threshold
Equipment required	Adjustment/verification fixture and fixture supply (item 4) Voltage reference (item 26) Precision BNC cable (item 31) Dual banana-to-BNC adapter (item 25) Capacitor, 0.1 µF (item 27)
Prerequisites	Warm-up time: 30 minutes for the TLA600 and test equipment Test equipment connected as shown in Figure 2–5 Diagnostics and SELF_CAL pass

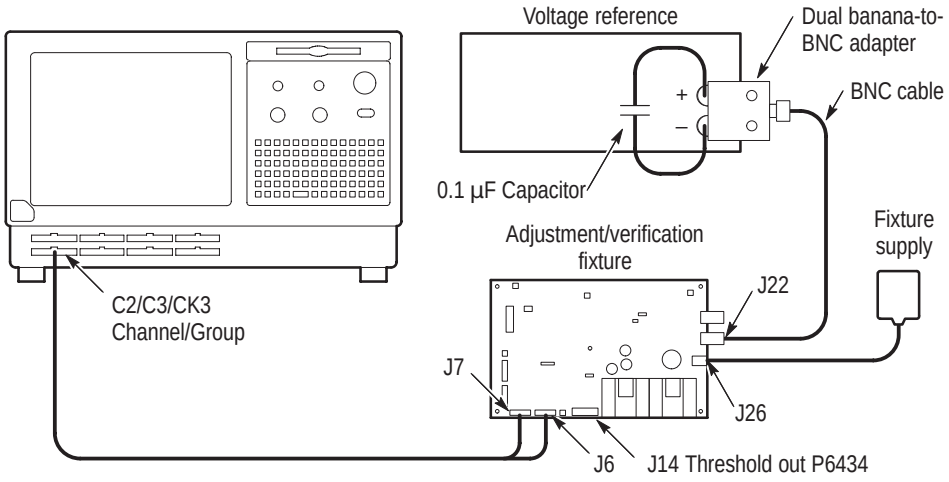


Figure 2–5: FPV_DC_Threshold test setup

1. If the logic analyzer application is running, quit the application.
2. Verify that all of the prerequisites listed previously are met for the procedure.
3. Run the PV/Adjust software as described in *Running the LA and DSO Software* on page 1–12. Run the C:\Tekcats\Tla_la, program, and select the correct options.
4. Follow the on-screen instructions to run each portion of the test for each parameter of the instrument.
5. Verify that all of the tests pass.

TLA600 Procedure 2: FPV_Setup_0F

This procedure verifies the setup time of the instrument.

SW test name	FPV_Setup_0F
Equipment required	Adjustment/verification fixture and fixture supply (item 4)
Prerequisites	Warm-up time: 30 minutes for the TLA600 and test equipment Test equipment connected as shown in Figure 2–6 Diagnostics and SELF_CAL pass

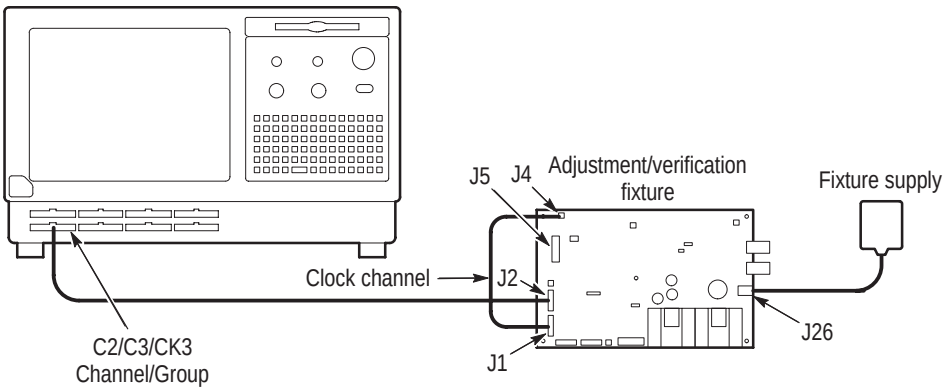


Figure 2–6: Initial FPV_Setup_0F test setup

1. If the logic analyzer application is running, quit the application and verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run each portion of the test for each parameter of the instrument.
3. Verify that all tests pass. If a test fails, run the Deskew routine as described in the *TLA600 Series Logic Analyzer Adjustment* section beginning on page 2–23, then rerun the test.

TLA600 Procedure 3: FPV_Hold_0F

This procedure verifies the hold time of the instrument.

SW test name	FPV_Hold_0F
Equipment required	Adjustment/verification fixture and fixture supply (item 4)
Prerequisites	Warm-up time: 30 minutes for the TLA600 and test equipment Test equipment connected as shown in Figure 2–7 Diagnostics and SELF_CAL pass

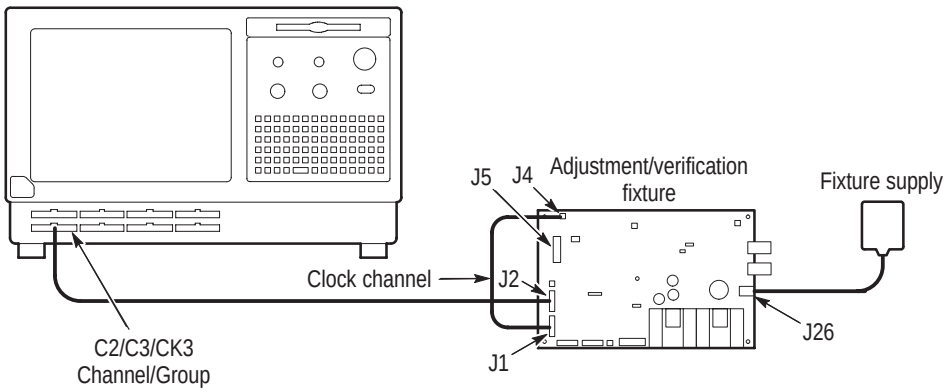


Figure 2–7: Initial FPV_Hold_0F test setup

1. If the logic analyzer application is running, quit the application and verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run the test for each channel on the system.
3. Verify that all tests pass. If a test fails, run the Deskew routine as described in the *TLA600 Series Logic Analyzer Adjustment* section beginning on page 2–23, then rerun the test.

TLA600 Procedure 4: FPV_Maxsync

This procedure checks the Maximum Synchronous Clock Rate and the Trigger State Sequence Rate. This test is performed once and applies to all channels of the instrument.

SW test name	FPV_Maxsync
Equipment required	Adjustment/verification fixture and fixture supply (item 4) Sine wave generator (item 33) BNC cable (item 31) Adapter, N-to-BNC (item 29)
Prerequisites	Warm-up time: 30 minutes for LA instrument and test equipment Test equipment connected as shown in Figure 2–8 Diagnostics and SELF_CAL pass

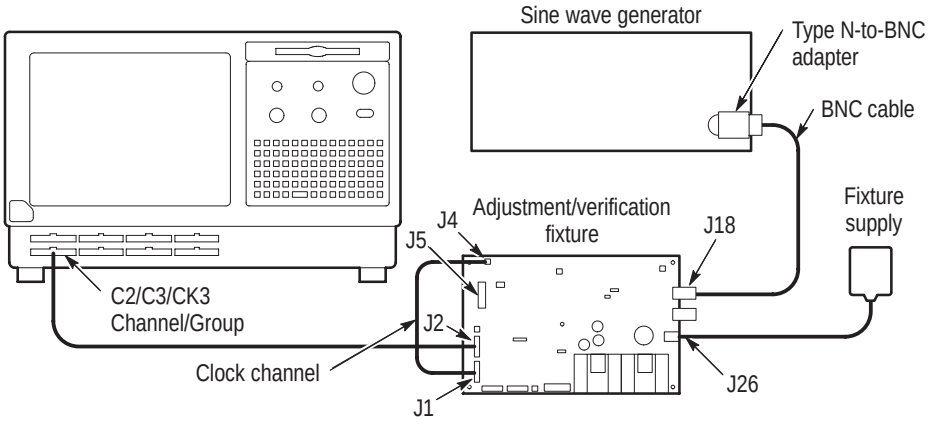


Figure 2–8: FPV_Maxsync test setup

1. If the TLA system application is running, quit the application and verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions.
3. Verify that all of the tests pass.

Completing the Performance Verification

After completing the performance verification procedures, obtain a copy of the test results and verify that all parameters are within the allowable specifications as listed in the *Tektronix Logic Analyzer Family User Manual*.

Refer to *Retrieving Test Data from the PV/Adjust Software* on page 1–15 for instructions on obtaining test data.

TLA600 Series Logic Analyzer Adjustment

This section contains procedures which use the PV/Adjust software to adjust the TLA600 Series Logic Analyzers to within factory specifications. The PV/Adjust software contains instructions and control programs for adjusting the logic analyzer. The software describes test equipment connections and settings, selects setup parameters, and loads calibration constants into memory.

These procedures adjust the logic analyzer for conformance with the warranted characteristics listed in the *Specifications* section of the *Tektronix Logic Analyzer Family User Manual*.

Adjustments should be done after repair or when performance verification test fail.

Prerequisites

These procedures ask for the serial number of the instrument under test. You can access the serial number through the logic analyzer application. In the application, go to the System menu, select System Properties, and click on the LA tab. However, you must quit the application before continuing with the PV/Adjust software procedures.

Only trained service technicians should perform this procedure after meeting the following requirements:

- The logic analyzer application must not be running.
- The PV/Adjust software must be loaded. Refer to *Software Installation and Removal Instructions* beginning on page 1–8.
- The logic analyzer requires a 30-minute warm-up time in a +20° C to +30° C environment before it is adjusted. Adjustments performed before the operating temperature has stabilized may cause errors in performance.

Using the Software

This section describes how to perform adjustments using the PV/Adjust software.

Performing the Adjustments

There are no manual adjustments for the logic analyzer. Instead, the PV/Adjust software adjusts the instrument hardware using external test equipment connections that you provide in response to prompts on the screen.

Upon successful completion of each adjustment, the PV/Adjust software automatically loads the new calibration data into memory.

Adjustment Sequences and Dependencies

The PV/Adjust software allows you to run groups of adjustments, or sequences. A sequence consists of one or more individual adjustments. Normally you will perform a RUN FULL SEQUENCE, which executes each adjustment in the proper order.

The PV/Adjust software also provides instructions for running each adjustment individually. However, you should only perform individual adjustments while troubleshooting.

Adjustment After Repair

You must perform a full adjustment sequence following replacement of any circuit board. Refer to the *Maintenance Section* of the *TLA600 Series Logic Analyzer Service Manual* for more details.

Test Equipment

In addition to the basic system setup, you will need some of the equipment shown in Table 1–3 on page 1–5 in the *Introduction* section.

Each procedure includes a table that calls out the equipment used. Use Table 1–3 to identify required equipment specifications. If you substitute equipment, always choose instruments that meet or exceed the minimum requirements specified.

Adjustment Instructions

This section describes how to perform adjustments using the PV/Adjust software.

Using the PV/Adjust Software

The PV/Adjust software contains instructions for performing the adjustments. The basic steps for completing the procedures follow:

1. Start the program, enter user and product identification information and temperature and humidity.
2. If you are using P6417 or P6418 probes, label one probe as the Reference Probe, and the other probe as the Probe Under Test.
3. If you are using a P6434 probe, label the probe channel group identified as the pin 38 side as Probe A. Label the probe channel group identified as the pin 1 side as Probe B, refer to Figure 2–9.

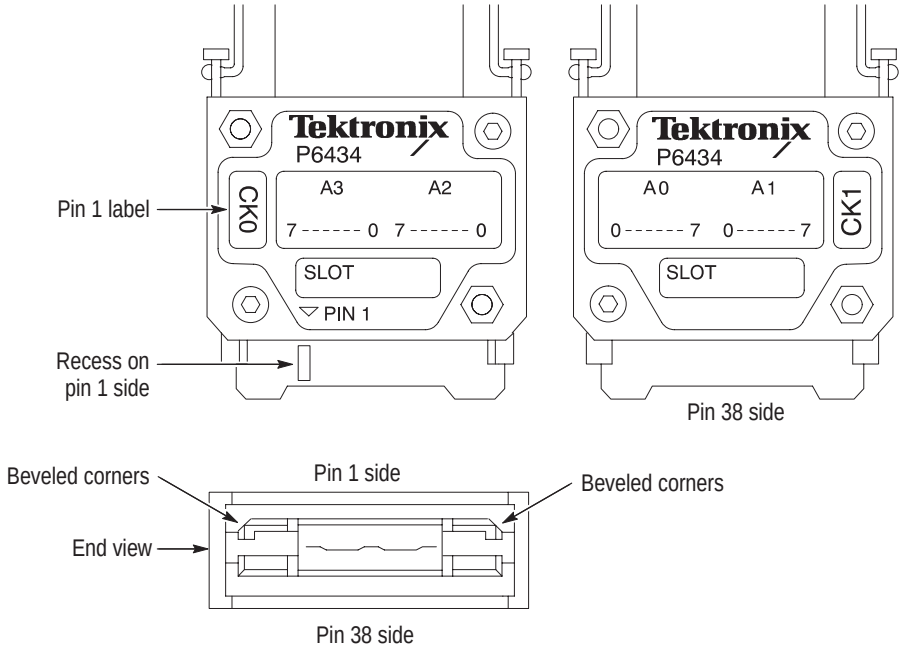


Figure 2–9: P6434 probe detail

4. Select a full adjustment sequence.
5. Connect the test equipment.
6. Set up the test equipment for the output signals described by on-screen instructions and by the connection illustration for each test.

7. Run each adjustment step as instructed by following the on-screen prompts.
8. After completing all the adjustment steps, view the results to confirm that the adjustment was successful.

Troubleshooting

If any adjustments fail, use the following steps to troubleshoot the problems:

- Check all test equipment for improper or loose connections.
- Check that all test equipment is powered on and has the proper warm-up time.
- Verify that the adjustment/verification fixture LED is lighted, the jumper positions match the on-screen instructions, and the external connections are correct.
- Rerun the diagnostics and self-cal.
- Run the adjustment procedures a second time to verify the failure.
- If the adjustment procedures continue to fail, refer to the *TLA 600 Series Logic Analyzer Service Manual* for corrective action.

Tests Performed

The adjustment procedures check and adjust the following parameters of the logic analyzer:

- SELF_CAL, an internal routine in the application software that adjusts acquisition thresholds, internal module and signal timing.
- Deskew, an adjustment routine in the PV/Adjust software which time-aligns all channels.

***NOTE**. Do not mix probe types (P6417, P6418 and P6434) when performing the deskew procedure.*

Adjustment Procedures

Refer to the following procedures to identify the initial setup for each adjustment. Then follow the program instructions to complete the adjustments.

Self Calibration

Self calibration (SELF_CAL) is an internal routine that optimizes performance at the current ambient temperature to maximize measurement accuracy. No external equipment or user actions are needed to complete the procedure. The logic analyzer saves data generated by the self calibration in memory. Passing the self calibration provides a higher level of confidence of functionality.

***NOTE**. Performing the self calibration does not guarantee that all parameters operate within limits.*

Operation within limits is achieved by performing the adjustment procedures.

Verification of operation within limits is accomplished by performing the performance verification procedures.

When to Perform the Self Calibration. You can run the self calibration at any time during normal operation. To maintain measurement accuracy, perform the self calibration if the following conditions occur:

- After repair and replacement of any circuit boards.
- It has been a year since the last self calibration was run

TLA600 Procedure 1: SELF_CAL

Perform the following steps to run the SELF_CAL routine. Before beginning this procedure, be sure that no active signals are applied to the instrument. Self calibration can fail if signals are applied to the probe during the procedure.

Prerequisites	Warm-up time: 30 minutes Power-up diagnostics pass

1. Ensure that the logic analyzer has had a 30-minute warm up before attempting the self calibration, and that the logic analyzer application is running.
2. Disconnect any probes connected to the logic analyzer.
3. Select the Calibration and Diagnostics property sheet from the System menu.
4. Select the Self Calibration tab.

5. Click the Run button to start the self calibration.

   The self calibration takes several minutes to complete, depending on the number of channels in the instrument. Upon successfully completing the self calibration, the status changes from Running to Calibrated, and the Date and Time field is set to the present.

TLA600 Procedure 2: Deskew

The deskew procedure is used to calibrate and adjust the timing alignment of the probe data channels and receivers.

Perform the deskew procedure:

- Once a year.
- If you have replaced the acquisition board (the probe constants are stored on the acquisition board).

This procedure checks and adjusts the time alignment of all channels. There are no manual adjustments.

SW test name	Deskew
Equipment required	Adjustment/verification fixture and fixture supply (item 4) Two P6417 or P6418 Logic Analyzer probes (item 8), OR One P6434 Logic Analyzer probe (item 9)
Prerequisites	Warm-up time: 30 minutes for the TLA600 and test equipment Test equipment connected as shown in Figure 2–10 Diagnostics and SELF_CAL pass

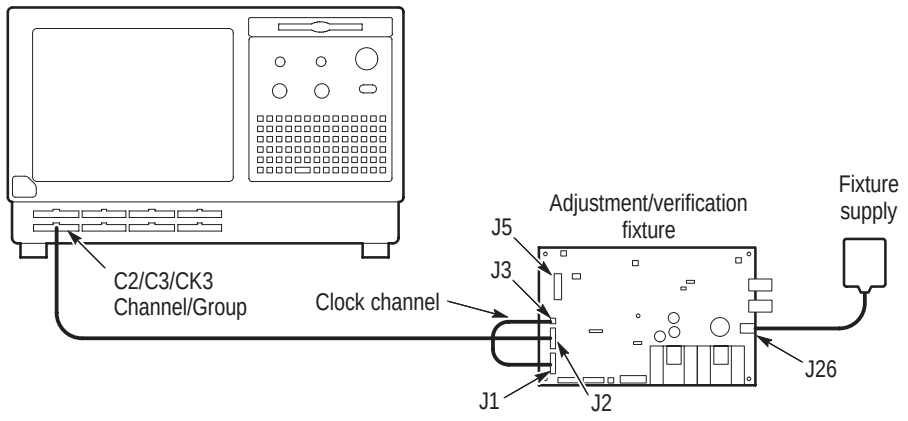


Figure 2–10: Initial deskew test setup

1. If the logic analyzer application is running, quit the application.
2. Verify that all of the prerequisites listed previously are met for the procedure.
3. Run the PV/Adjust software as described in the *Running the LA and DSO Software* on page 1–12. Run the C:\Tekcats\Tla_la program and select the correct options.

***NOTE**. These procedures assume that a P6418 or P6417 probe is being used. If you are using a P6434 probe, use J5, the Data Out connector on the adjustment/ verification fixture for performing the deskew test. Observe proper polarity: pin 1 to pin 1.*

---

4. Follow the on-screen prompts to perform the adjustment procedure.
5. Verify no failures occur for each test.

If desired, you can print or save the results of the deskew adjustment operation. However, this is not required for calibration. The file will be over written when the next adjustment or performance verification sequence is run.

If failures do occur, confirm that diagnostics and SELF_CAL pass.

Completing the Adjustment Steps

After completing the adjustments, obtain a copy of the test results and verify that all tests passed. Refer to *Retrieving Test Data from the PV/Adjust Software* on page 1–15 for instructions on obtaining test data.

Run the *Performance Verification Procedures* to verify that the all parameters are within the allowable specifications as listed in the *Tektronix Logic Analyzer Family User Manual.*

Portable Mainframe

Portable Mainframe Functional Verification

This section contains instructions for performing the functional verification of the TLA704 Portable Mainframe and the TLA714 Portable Mainframe.

Tests Performed

Table 3–1 lists the functional verification procedures that are available for the Portable Mainframe.

Table 3–1: Functional verification procedures

Instrument	Procedure
Portable Mainframe	Power-up diagnostics
Portable Mainframe	Extended diagnostics
Portable Mainframe	TLA700 Mainframe diagnostics
TLA704 Portable Mainframe	QAPlusWin diagnostics[1]
TLA714 Portable Mainframe	QA+Win32 diagnostics[1]

[1] **The version of QAPlus diagnostics may vary depending on your instrument. Refer to the online notes or Readme files for more information.**

NOTE*. Running the extended diagnostics will invalidate any acquired data. If you want to save any data, do so before running the extended diagnostics.*

Test Procedure

You will need a Portable Mainframe with an LA or DSO module installed.

Equipment required	Cable, 50 Ω coaxial (item 31)
Prerequisites	Warm-up time: 30 minutes

Perform the following tests to complete the functional verification procedure.

Extended Diagnostics

Do the following steps to run the extended diagnostics:

1. Power on the instrument and wait for the logic analyzer application to start.
2. Go to the System menu and select Calibration and Diagnostics.
3. Verify that all power-on diagnostics pass.
4. Click the Extended Diagnostics tab.
5. Select All Modules, All Tests and then click the Run button on the property sheet.

   All tests that displayed an “Unknown” status will change to a Pass or Fail status depending on the outcome of the tests.
6. Scroll through the tests and verify that all tests pass.

TLA700 Mainframe Diagnostics

The TLA700 Mainframe Diagnostics are a comprehensive software test that checks the functionality of the portable mainframe. To run the TLA700 Mainframe Diagnostics, do the following steps:

1. Quit all other applications.
2. Click the Windows Start button.
3. Select Programs from the Start menu.
4. Select Tektronix TLA700 from the Programs menu.
5. Select Tektronix TLA700 Mainframe Diagnostics from the Tektronix TLA700 menu.
6. Run the mainframe diagnostics.

***NOTE**. If modules are installed in the mainframe when the TLA700 Mainframe Diagnostics run, a Mainframe Diagnostics Warning dialog box appears. Clicking OK will initiate a SYSRESET, which will invalidate any acquired data in the modules. You may want to save acquired data before continuing.*

QAPlusWin or QA+Win32

QAPlusWin and QA+Win32 are comprehensive software applications used to check and verify the operation of the PC hardware. To run the software, you must have either a keyboard, mouse, or other pointing device.

***NOTE**. Before running the QAPlus tests, check the release notes to become aware of possible problems and workarounds.*

To run software, follow these instructions:

1. Quit all other applications.
2. Click the Windows Start button.
3. Select the QA+Win32 or QAPlusWin software.
4. Run the diagnostics.

Cooling Fan Operation

Power on the instrument and inspect the rear of the instrument to verify that all six cooling fans are rotating.

Portable Mainframe Certification

The system clock is checked for accuracy. The instrument is certifiable if this parameter meets specifications. Do the performance verification procedures and record the values on the Calibration Data Report provided on the following pages.

Calibration Data Report

TLA 704 Color Portable Mainframe

Instrument model number: _____

Serial number: _____ Certificate number: _____

Verification performed by: _____ Verification date: _____

System Clock Test Data

Characteristic	Specification	Tolerance	Procedure reference	Incoming data	Outgoing data
Clock frequency	10 MHz	±1 kHz (9.9990 MHz-10.0010 MHz)	Page 3–14, Step 5		

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Calibration Data Report

TLA 714 Color Portable Mainframe

Instrument model number: _____

Serial number: _____ Certificate number: _____

Verification performed by: _____ Verification date: _____

System Clock Test Data

Characteristic	Specification	Tolerance	Procedure reference	Incoming data	Outgoing data
Clock frequency	10 MHz	±1 kHz (9.9990 MHz-10.0010 MHz)	Page 3–14, Step 5		

Tektronix

Portable Mainframe Performance Verification

This section contains procedures to verify that the TLA704 Portable Mainframe and the TLA714 Portable Mainframe perform as warranted. Verify instrument performance whenever the accuracy or function of your instrument is in question, or as part of an annual calibration/certification.

Tests Performed

Table 3–2 lists the performance verification procedures available for the Portable Mainframe. The procedures are identical for both the TLA704 Portable Mainframe and the TLA714 Portable Mainframes.

Table 3–2: Performance verification procedures

Parameter	Procedure
Power supply voltages	Voltage level check
System clock (CLK10)[1]	Signal output check

1 **Certifiable parameter**

Test Procedures

Use the following steps to complete the performance verification procedure. You will need some of the equipment shown in Table 1–3 on page 1–5 to complete the performance verification procedures. If you substitute equipment, always choose instruments that meet or exceed the minimum requirements specified.

Checking Power Supply Voltages

Do the following to verify power supply performance:

Equipment required	DMM with test leads (item 24) Two miniature probe-to-square pin adapters (item 22) 0.025-inch square pin (item 23) Frequency counter (item 15) Precision BNC cable (item 31)
Prerequisites	Warm-up time: 30 minutes for the portable mainframe and test equipment Power-on, mainframe, and QA+WIN32 diagnostics pass

1. Power off the portable mainframe and remove any modules installed in it.
2. Power on the portable mainframe and connect the reference lead of a digital voltmeter to chassis ground, such as the top of the power supply.
3. Attach a 0.025-inch square pin to the probe tip of the other lead and insert it into one of the pins on the backplane connectors listed in Table 3–3.

CAUTION. *Use of a square pin of other dimensions will damage the Portable Mainframe.*

The pins that should be carrying voltages are listed in Table 3–3. The arrangement of J1 and J2 connectors on the backplane is shown in Figure 3–1. Measure the power supply voltages with the voltmeter and compare each reading to the values listed in the tables. If the voltages are within the ranges listed in the table, the power supply is operating properly.

Table 3–3: Power supply voltages and backplane connector pins

J1 pin	Voltage (range)	J2 pin	Voltage (range)
Row A		Row A	
31	–12 V (–12.60 V to –11.64 V)	2	–2 V (–2.10 V to –1.90 V)
		25	+5 V (4.875 V to 5.250 V)
Row C		Row C	
31	+12 V (11.64 V to 12.60 V)	4	–5.2 V (–5.460 V to –5.044 V)
		31	+24 V (23.28 V to 25.20 V)
		32	–24 V (–25.20 V to –23.28 V)

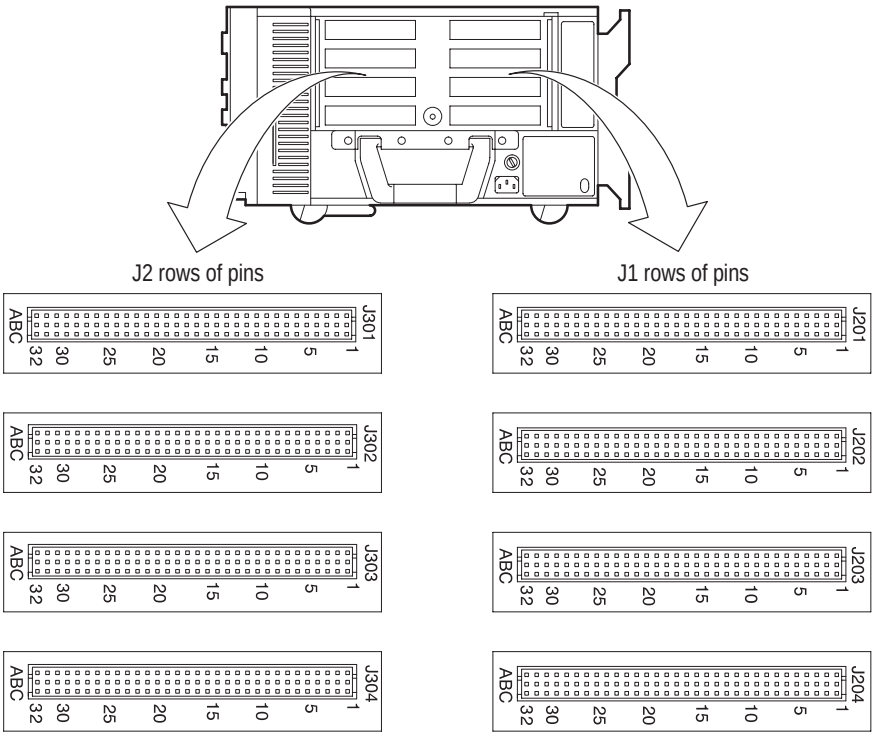

Figure 3–1: Location of J1 and J2 pins in the portable mainframe

Checking the 10 MHz System Clock (CLK10)

Do the following to check the accuracy of the system clock.

1. Connect the frequency counter to the External Signal Out TTL BNC connector on the rear of the portable mainframe.
2. Verify that the logic analyzer application is running.
3. Go to the System window and select System Configuration from the System menu.
4. In the System Configuration dialog box, select 10 MHz Clock from the list of routable signals in the External Signal Out selection box and click OK.
5. Verify that the output frequency at the External Signal Out TTL connector is 10 MHz ±1 kHz. Record the measurement on the Calibration Data Report.
6. In the system configuration dialog box, reset the External Signal Out signal to None.
7. Disconnect the frequency counter and power off the portable mainframe.
8. Reinstall any modules that were removed at the beginning of the performance verification procedure.

Portable Mainframe Adjustment

There are no adjustments for the TLA704 Portable Mainframe or the TLA714 Portable Mainframe.

Benchtop Chassis and Expansion Mainframe

Benchtop Chassis and Expansion Mainframe Functional Verification

This section contains instructions for performing the functional verification of the TLA711 Benchtop Chassis, the TLA720 Benchtop Chassis and the TLA7XM Expansion Mainframe (with an expansion module). Because these products are basically identical the functional checks are the same for both products.

Benchtop Chassis

Power on the benchtop chassis and observe that the On/Standby switch illuminates. Verify that the fan spins without undue noise.

Expansion Chassis

Ensure that you have an expansion module installed in the expansion mainframe. Refer to the *TLA700 User Manual* for installation information if necessary.

The expansion mainframe automatically powers on when the attached benchtop or portable mainframe powers on. If everything is properly connected and operational, you should see the expansion mainframe and the installed modules in the System window.

Observe that the On/Standby switch illuminates. Verify that the fan spins without undue noise.

Benchtop Chassis and Expansion Mainframe Certification

There are no certifiable parameters for the TLA711 Benchtop Chassis, the TLA720 Benchtop Chassis, and for the TLA7XM Expansion Mainframe. There are also no certifiable parameters for the expansion module.

Benchtop Chassis and Expansion Mainframe Performance Verification

This section contains procedures to verify that the TLA711 Benchtop Chassis, the TLA720 Benchtop Chassis, and the TLA7XM Expansion Mainframe (with the expansion module) perform as warranted. Verify instrument performance whenever the accuracy or function of your instrument is in question.

NOTE. *There are no certifiable parameters on the TLA711 Benchtop Chassis, the TLA720 Benchtop Chassis, or for the TLA7XM Expansion Mainframe and expansion module. Refer to the benchtop controller for certification requirements for the chassis.*

Test Procedure

Do the following tests to verify the performance of the benchtop chassis or the expansion mainframe. You will need some of the equipment shown in Table 1–3 on page 1–5 to complete the performance verification procedures. If you substitute equipment, always choose instruments that meet or exceed the minimum requirements specified.

Check Power Supply Voltages

Use a digital voltmeter to check the voltages on the pins of the 25-pin connector and compare the results against the range listed in Table 4–1. The connector is located on the right rear panel of the chassis (see Figure 4–1).

Equipment required	Digital multimeter with test leads (item 24) Two 0.025-inch square pins (item 23) Two miniature probe-to-square pin adapters (item 22)
Prerequisites	Warm-up time: 30 minutes

CAUTION. *To prevent damaging the 25 pin connector, use care when probing the connector with the square pins.*

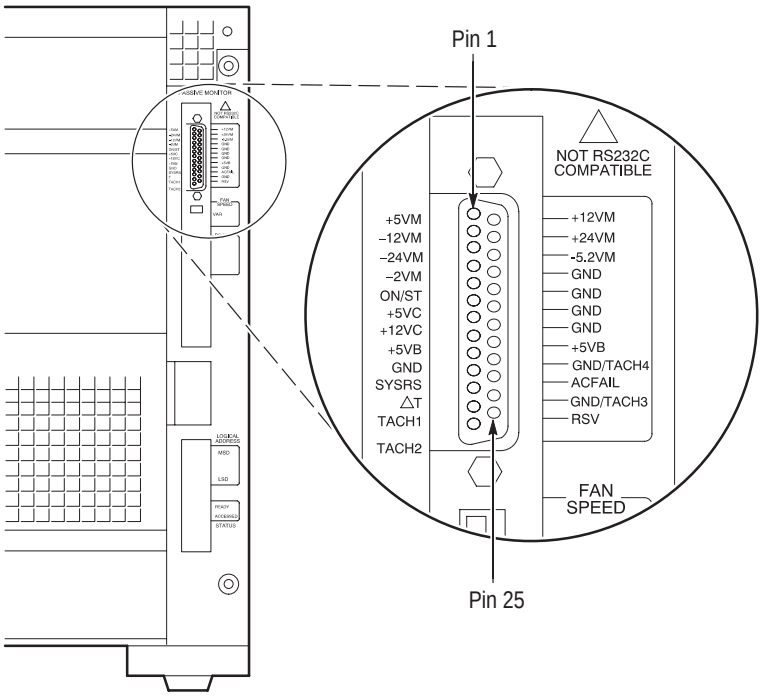

Figure 4–1: Benchtop and Expansion Chassis 25-pin rear panel connector

1. Connect the reference lead of the digital voltmeter to one of the ground pins.
2. Connect the other lead of the digital voltmeter to the supply pins of the 25-pin connector on the right rear panel of the chassis.
3. Measure the power supply voltages with the voltmeter and compare each reading to the values listed in Table 4–1. If the voltages are within the specified ranges, your chassis is operating properly.

Table 4–1: Power supply voltages at the 25-pin connector

Pin	Supply	Acceptable voltage range
1	+5 V	4.875 V to 5.250 V
2	–12 V	–12.60 V to –11.64 V
3	–24 V	–25.20 V to –23.28 V
4	–2 V	–2.10 V to –1.90 V
14	+12 V	11.64 V to 12.60 V
15	+24 V	23.28 V to 25.20 V
16	–5.2 V	–5.460 V to –5.044 V
9, 17–20, 22, 24	Logic Ground	

Benchtop Chassis and Expansion Mainframe Adjustment

There are no adjustments for the TLA711 Benchtop Chassis, the TLA720 Benchtop Chassis and the TLA7XM Expansion Mainframe (and expansion module).

Benchtop Controller

Benchtop Controller Functional Verification

This section contains instructions for performing the TLA711 Benchtop Controller and TLA720 Benchtop Controller functional verification procedures.

Tests Performed

Table 5–1 lists the functional verification procedures available for the benchtop controller. The procedures are identical for both versions of benchtop controllers except where noted.

Table 5–1: Functional verification procedures

Instrument	Procedure
Benchtop Controller	Power-up diagnostics
Benchtop Controller	Extended diagnostics
Benchtop Controller	TLA700 Mainframe diagnostics
TLA711 Benchtop Controller	QAPlusWin diagnostics[1]
TLA720 Benchtop Controller	QA+Win32 diagnostics[1]

[1] **The version of QAPlus diagnostics may vary depending on your instrument. Refer to the online notes or Readme files for more information.**

NOTE. *Running the extended diagnostics will invalidate any acquired data. If you want to save any data, do so before running the extended diagnostics.*

Test Procedure

You will need a benchtop chassis with an LA module or DSO module installed.

Equipment Required	Cable, 50 Ω coaxial (item 31)
Prerequisites	Warm-up time: 30 minutes

Extended Diagnostics

Do the following steps to run the extended diagnostics:

1. Power on the instrument and wait for the logic analyzer application to start.

2. Go to the System menu and select Calibration and Diagnostics.
3. Verify that all power-on diagnostics pass.
4. Click the Extended Diagnostics tab.
5. Select All Modules, All Tests and then click the Run button on the property sheet.

   All tests that displayed an "Unknown" status will change to a Pass or Fail status depending on the outcome of the tests.
6. Scroll through the tests and verify that all tests pass.

TLA700 Mainframe Diagnostics

The TLA700 Mainframe Diagnostics are a comprehensive software test that checks the functionality of the instrument. To run the TLA700 Mainframe Diagnostics, do the following steps:

1. Quit all other applications.
2. Click on the Windows Start button.
3. Select Programs from the Start menu.
4. Select Tektronix TLA700 from the Programs menu.
5. Select Tektronix TLA700 Mainframe Diagnostics from the Tektronix TLA700 menu.
6. Run the mainframe diagnostics.

NOTE. *If modules are installed in the mainframe when the TLA700 Mainframe Diagnostics are run, a Mainframe Diagnostics Warning dialog box appears. Clicking OK will initiate a SYSRESET, which will invalidate any acquired data in the modules. You may want to save acquired data before continuing.*

QAPlus Software

QAPlusWin and QA+Win32 are comprehensive software applications used to check and verify the operation of the PC hardware. To run the software, follow these instructions:

1. Quit all other applications.
2. Click the Windows Start button.
3. Select the QA+Win32 or QAPlusWin software.
4. Run the diagnostics.

Benchtop Controller Certification

The system clock is checked for accuracy. The instrument is certifiable if this parameter meets specifications. The procedure is described in the *Performance Verification* section. Record the results in the appropriate Calibration Data Report on the following pages.

Calibration Data Report

TLA711 Color Benchtop Controller

Instrument model number: _____

Serial number: _____ Certificate number: _____

Verification performed by: _____ Verification date: _____

System Clock Test Data

Characteristic	Specification	Tolerance	Procedure reference	Incoming data	Outgoing data
Clock frequency	10 MHz	±1 kHz (9.9990 MHz-10.0010 MHz)	Page 5–10, Step 5		

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Calibration Data Report

TLA720 Color Benchtop Controller

Instrument model number: _____

Serial number: _____ Certificate number: _____

Verification performed by: _____ Verification date: _____

System Clock Test Data

Characteristic	Specification	Tolerance	Procedure reference	Incoming data	Outgoing data
Clock frequency	10 MHz	±1 kHz (9.9990 MHz-10.0010 MHz)	Page 5–10, Step 5		

Tektronix

Benchtop Controller Performance Verification

This section contains procedures to verify that the TLA711 Benchtop Controller and the TLA720 Benchtop Controller performs as warranted. Verify instrument performance whenever the accuracy or function of your instrument is in question.

Tests Performed

Table 5–2 lists the performance verification procedures available for the Benchtop Controller. The procedures are identical for the TLA711 Benchtop Controller and the TLA720 Benchtop Controller.

Table 5–2: Performance verification procedures

Parameter	Procedure
System clock (CLK 10)[1]	10 MHz system clock test

1 Certifiable parameter

Test Procedures

Perform the following steps to complete the performance verification procedure. You will need some of the equipment shown in Table 1–3 on page 1–5 to complete the performance verification procedures. If you substitute equipment, always choose instruments that meet or exceed the minimum requirements specified

The following procedure checks the accuracy of the 10 MHz system clock.

Equipment required	Frequency counter (item 15) SMB-to-BNC cable (item 20)
Prerequisites	Warm-up time: 30 minutes Power-up, mainframe, and QA+WIN32 diagnostics pass

1. Verify that all of the prerequisites above are met for the procedure.
2. Connect the frequency counter to the External Signal Out TTL SMB connector on the benchtop controller.

3. Go to the System window and select System Configuration from the System menu.
4. In the System Configuration dialog box, select 10 MHz Clock from the list of routable signals in the External Signal Out selection box and click OK.
5. Verify that the output frequency at the External Signal Out TTL connector is 10 MHz ±1 kHz. Record the measurement on the Calibration Data Report and disconnect the frequency counter.
6. In the System Configuration dialog box, reset the External Signal Out signal to None.

Benchtop Controller Adjustment

There are no adjustments for the TLA711 or TLA720 benchtop controller.

Logic Analyzer Module

Logic Analyzer Module Functional Verification

This section contains instructions for performing the functional verification procedures for the TLA7Lx, TLA7Mx, TLA7Nx, TLA7Px, and TLA7Qx Logic Analyzer modules. These procedures provide an easy way to check the basic functionality of the LA modules and probes.

Table 6–1 lists the functional verification procedures available for the TLA 700 Series Logic Analyzer modules and probes.

Table 6–1: Logic Analyzer Module functional verification procedures

Instrument	Procedure	Adjustment/verification fixture required
Single logic analyzer module	Extended diagnostics	No
Merged logic analyzer module	Extended diagnostics	No
	Merge diagnostics	No
P6417, P6418, and P6434 Logic Analyzer probe	Signal input check	Yes

If any check within this section fails, refer to the *Troubleshooting* chapter in the *TLA7Nx, TLA7Px, and TLA7Qx Logic Analyzer Module Service Manual* for assistance. Failed tests indicate the instrument needs to be serviced.

The functional verification procedure consists of the following parts:

- Module self tests and power-on diagnostics
- Single module procedure
- Merged module procedure
- Probe verification

This procedure provides a functional check only. If more detailed testing is required, perform the *Performance Verification Procedure* after completing this procedure.

Perform these tests whenever you need to gain confidence that the instrument is operating properly.

Test Equipment

You will need the following equipment to complete the functional verification procedure:

- TLA 700 Series Logic Analyzer mainframe with one LA module installed (more modules are required to check the merged functionality)
- One adjustment/verification fixture with power supply

Setup

It is assumed that the LA module is properly installed and that all accessories are connected. Refer to the *TLA 700 Series Logic Analyzer User Manual* for installation instructions.

Power on the instrument and allow a 30-minute warmup before continuing with any procedures in this section.

Module Self Tests and Power-On Diagnostics

During power-on, the installed modules perform an internal self test to verify basic functionality. No external test equipment is required. The self tests require only a few seconds per module to complete. The front-panel ARM'D and TRIG'D indicators blink during the self test. After testing completes, the front panel indicators have the following states:

- READY — Green (on)
- ACCESSED — off
- ARM'D — off
- TRIG'D — off

Next, the power-on diagnostics are run. If any self tests or power-on diagnostics fail, the instrument displays the Calibration and Diagnostics property sheet.

Single LA Module Functional Verification Procedure

The following procedure checks the basic functionality of a single LA module. Functional verification consists of running the extended diagnostics.

***NOTE**. Running the extended diagnostics invalidates any acquired data. If you want to save any of the acquired data, do so before running the extended diagnostics.*

Prerequisites	Warm-up time: 30 minutes Power-up diagnostics pass SELF_CAL passes

Perform the following steps to complete the functional verification procedures. Before beginning this procedure, be sure that no active signals are applied to the instrument. Certain diagnostic tests will fail if signals are applied to the probe during the test.

1. In the logic analyzer application, go to the System menu and select Calibration and Diagnostics.
2. Click the Extended Diagnostics tab.
3. Select the top level test and click the Run button.

   The diagnostics will perform each one of the tests listed in the menu under the module selection. All tests that displayed an Unknown status will change to a Pass or Fail status depending on the outcome of the tests.
4. Scroll through the test results and verify all tests pass.

***NOTE**. If Extended Diagnostics fail, run Self Cal for the LA module and then rerun Extended Diagnostics.*

Merged LA Module Functional Verification Procedure

The following procedure checks the basic operation of the merged modules. If necessary, refer to the *TLA 700 Series Logic Analyzer User Manual* for instructions on merging LA modules.

***NOTE**. Running the extended diagnostics will invalidate any acquired data. If you want to save any of the acquired data, do so before running the extended diagnostics.*

Prerequisites	Warm-up time: 30 minutes
	Merge cable installed between all of the LA merged modules
	Power-up diagnostics pass
	SELF_CAL passes

Perform the following steps to complete the functional verification procedures. Before beginning this procedure, be sure that no active signals are applied to the instrument. Certain diagnostic tests will fail if signals are applied to the probe during the test.

1. In the logic analyzer application, go to the System menu and select Calibration and Diagnostics.
2. Click the Extended Diagnostics tab.
3. Select the top level test and click the Run button.

   The diagnostics will perform each one of the tests listed in the menu under the module selection. All tests that displayed an Unknown status will change to a Pass or Fail status depending on the outcome of the tests.
4. Scroll through the test results and verify all tests pass.

***NOTE**. If Extended Diagnostics fail, run Self Cal for the LA modules and then rerun Extended Diagnostics.*

Logic Analyzer Probe Functional Verification Procedure

The following procedure checks the basic operation of the probes by verifying that the probes recognize signal activity at the probe tips.

Equipment required	Adjustment/verification fixture version (item 4)
Prerequisites	Warm-up time: 30 minutes P6417, P6418 or P6434 probe connected[1] Test equipment connected as shown in Figure 6–1 Diagnostics and SELF_CAL pass

1 **Do not mix probes; only one type of probe can be functionally verified at a time.**

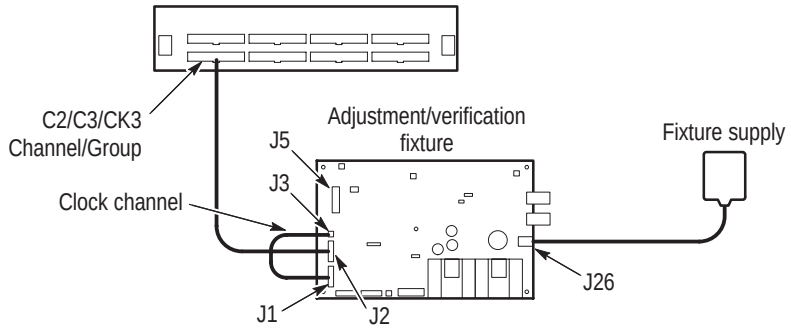

Figure 6–1: Probe functional verification test setup

Test Procedure

Perform the following steps to complete the probe functional verification:

1. Ensure that the jumper at J15 on the adjustment/verification fixture is in the INT position to select the internal 50.065 MHz clock. See Figure 6–4 on page 6–14 for location of J15.
2. Open the Setup window for the LA module.
3. Click the Set Thresholds button to display the Probe Threshold dialog box.
4. Adjust the threshold level to 700 mV for all channels.
5. Connect the acquisition probe to be tested to the C3/C2 channel group on the LA module.
6. Refer to Figure 6–1 and connect the probe to J1 and J2 on the adjustment/verification fixture. Ensure that you connect the ground side of the podlets to the ground side of the adjustment/verification fixture connectors.

***NOTE**. These procedures assume the P6418 or P6417 probes are being used. If you have a P6434 probe, use J5, the Data Out connector on the adjustment/verification fixture for verifying probe functionality. Observe proper polarity: pin 1 to pin 1.*

7. Connect the single clock (CK n) or the qualifier (Q n) channel to one of the J3 CLK OUT connector pairs on the adjustment/verification fixture.
8. Return to the Setup window and click the Show Activity button to display the Activity Monitor.
9. Verify that the Activity Monitor shows activity on all probe channels connected to the test fixture.

   Figure 6–2 shows an example of the Activity Monitor. Note the signal activity for clock CK3 and data channels for the C3(7-0) and C2(7-0) groups. Also note that there is no activity on the other groups because the probe podlets are not connected to a signal source (the channels are all high).

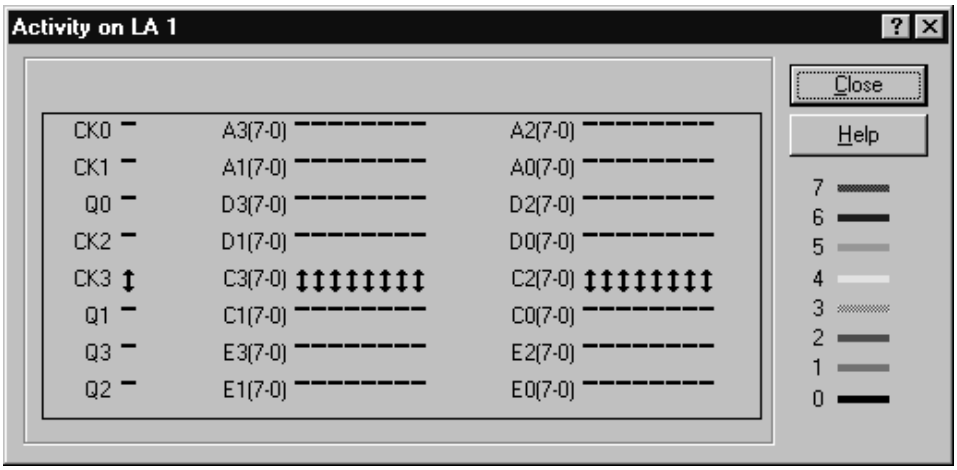

Figure 6–2: Activity Monitor

10. Verify that none of the connected channels are stuck high or stuck low.
11. Disconnect the probe from the adjustment/verification fixture and module.
12. Repeat steps 5 through 11 for any remaining probes.
13. Close the Activity Monitor.
14. Return the threshold levels to their former values in the Probe Threshold window.

Logic Analyzer Module Certification

Using the performance verification procedures, perform the DC Threshold test and print the software-generated Calibration Data Report. Other module specifications can also be verified by running the performance verification procedures.

Logic Analyzer Module Performance Verification

This section contains procedures to verify that the TLA7Lx, TLA7Mx, TLA7Nx, TLA7Px, and TLA7Qx modules perform as warranted. Verify instrument performance whenever the accuracy or function of your instrument is in question, or as part of an annual calibration/certification.

As a general rule, these tests should be done once a year.

Prerequisites

These procedures ask for the serial number of the LA module under test. Before installing the LA module in the mainframe, record the serial number and state speed of the LA module.

Alternatively, you can access the module serial number and state speed through the logic analyzer application. In the application, go to the System menu, select System Properties, and then click the LA module tab. However, you must quit the logic analyzer application before continuing with the performance verification procedures.

The tests in this section comprise an extensive, valid confirmation of performance and functionality when the following requirements are met:

- When multiple LA modules of the same model number are installed in the mainframe, the PV/Adjust software will address only the module in the highest-numbered slot.

  If you are testing a TLA7Q4 module for example, move it to a higher slot number than all other TLA7Q4 modules in the mainframe. This method avoids unnecessary module warm-up time.

- When verifying the performance of merged modules using the same type of individual modules, the individual modules must be physically separated before continuing; refer to the *TLA 700 Series Logic Analyzer User Manual* for information on merging and unmerging modules.

- The logic analyzer application must not be running.

- The PV/Adjust software must be loaded. Refer to *Software Installation and Removal Instructions* on page 1–8.

- The LA module must be installed in a mainframe, operating for at least 30 minutes, and operating at an ambient temperature between +20° C and +30° C.

- The LA module must have been last adjusted at an ambient temperature between +20° C and +30° C.
- The logic analyzer must be in an operating environment within the limits described in the *Specifications* section of the *TLA 700 Series Logic Analyzer User Manual*.

Merged Modules

When verifying the performance of merged modules consisting of different types of individual modules, the merged module can be tested without separation.

The PV/Adjust software runs independent of the logic analyzer application and does not recognize configuration settings. It is unnecessary to unmerge modules through the logic analyzer application before performing these procedures.

Tests Performed

The PV/Adjust software contains the tests shown in Table 6–2. Each test verifies one or more parameters. All of the tests check characteristics that are designated as checked (✓) in the *Specifications* section of the *Tektronix Logic Analyzer Family User Manual.* By running a full PV sequence, you will verify the performance of the LA Module.

Table 6–2: LA Module performance verification tests

Performance verification test name	Specification tested
1. FPV_DC_THRESHOLD[1]	Threshold accuracy
2. FPV_SETUP_0F	Setup time
3 FPV_HOLD_0F	Hold time
4. FPV_MAXSYNC	Maximum synchronous clock rate

[1] **Certifiable parameter**

Table 6–3 lists the additional characteristics that are designated as checked (✓) in the *Specifications* section of the *Tektronix Logic Analyzer Family User Manual*. These characteristics are indirectly tested by the PV/Adjust software tests named in the table.

Table 6–3: LA Module characteristics indirectly checked by the performance verification tests

Performance verification test name	Specification tested
1. FPV_SETUP_0F	Minimum recognizable word[1,2]
2 FPV_HOLD_0F	Minimum recognizable word[1,2]
3. All tests	Trigger state sequence rate
4. All tests, and Extended Diagnostics	Internal sampling period[3]

1 **When the setup and hold time tests are both performed, the setup and hold window size is indirectly verified.**

2 **When the setup and hold time tests are both performed, the channel-to-channel skew is indirectly verified.**

3 **When all of the tests are performed, including Extended Diagnostics, the internal sampling period is indirectly verified.**

Test Equipment

These procedures use external, traceable signal sources to directly test the characteristics that are designated as checked (✓) in the *Specifications* section of the *Tektronix Logic Analyzer Family User Manual.*

In addition to the basic system setup, you will need some of the equipment shown in Table 1–3 on page 1–5 to complete the performance verification procedures.

Each procedure includes a table that calls out the equipment used. Use Table 1–3 for equipment specifications. If you substitute equipment, always choose instruments that meet or exceed the minimum requirements specified.

Using the Software

This section provides a brief overview on using the PV/Adjust software.

When using the PV/Adjust software, you will connect external test equipment to the LA module in response to prompts on the screen. You will connect the test signals and then instruct the program to continue. The PV/Adjust software automatically selects the module settings and determines the results of each test.

The results of the tests are recorded in a temporary file and are available upon test completion for completing test records for certification. To obtain partial test information you can also run individual tests or selected groups.

NOTE. *The SELF_CAL test must run successfully before the other tests are performed. The remaining tests can then be performed in any order.*

Before testing an instrument following repair, you must first complete the adjustment procedure.

The PV/Adjust software contains online instructions for performing the performance verification procedure. The basic steps for completing the procedures follow:

1. Start the program, enter user and product identification information, temperature, and humidity.
2. If you are using P6417 or P6418 probes, label one probe as the Reference Probe, and the other probe as the Probe Under Test.
3. If you are using a P6434 probe, label the probe channel group identified as the pin 38 side as Probe A. Label the probe channel group identified as the pin 1 side as Probe B; refer to Figure 6–3.
4. Select a full test sequence.
5. Connect the test equipment.
6. Set up the test equipment for the output signals described by on-screen instructions and by the connection illustration for each test.
7. Run each test as instructed.

NOTE. *Some tests prompt you for input on whether to "1:Do Section or 2:Skip Section". It is recommended that you select "Do Section," unless you use the software for troubleshooting.*

8. After completing all the tests, view the test results and print them out if performing a certification. Refer to *Retrieving Test Data from the PV/Adjust Software* on page 1–15 for instructions on obtaining test data.

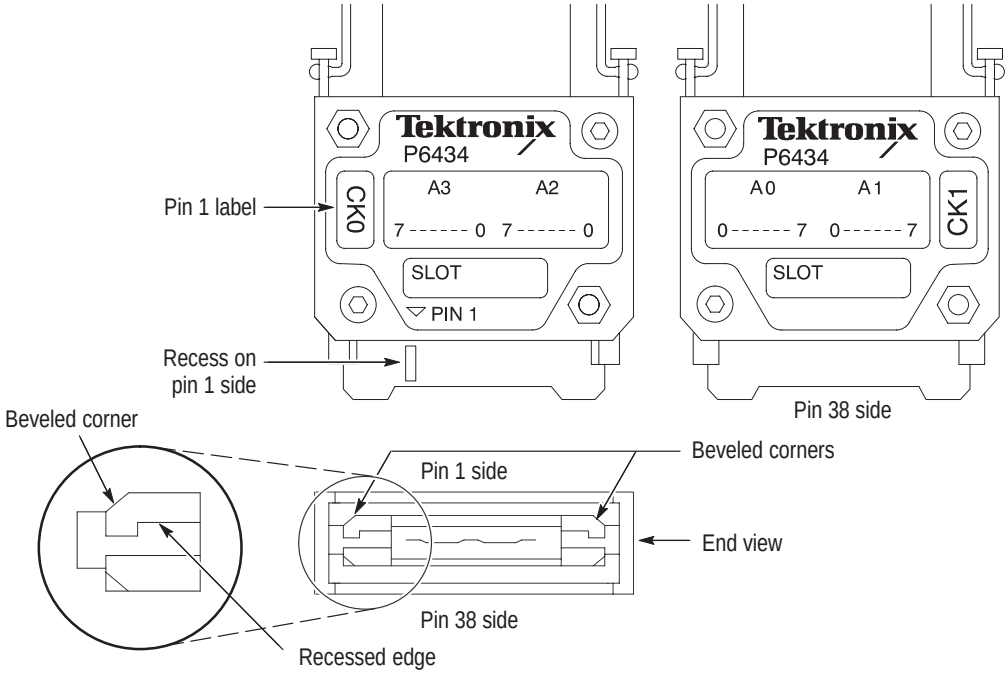

Figure 6–3: P6434 probe detail

Troubleshooting

If any tests fail, use the following steps to troubleshoot problems:

1. Check all test equipment for improper or loose connections.
2. Check that all test equipment is powered on and has the proper warm-up time.
3. If you are using the adjustment/verification fixture, verify the LED is lighted, the jumper positions match the on-screen instructions, and the external connections are correct. (See Figure 6–4 for jumper locations.)
4. Rerun mainframe or module diagnostics and module adjustment.
5. Run the tests a second time to verify the failure.
6. If tests continue to fail, refer to the *TLA 7Mx/TLA 7Lx Series Logic Analyzer Module Service Manual* for corrective action.

Performance Verification Tests

Use the following tables and figures to set up and execute each procedure.

NOTE. *The illustrations in the following procedures show P6418 or P6417 probes. If you have a P6434 probe, use J14 on the adjustment/verification fixture for the DC Threshold test; all other procedures using the P6434 probe use J5, the Data Out connector. When using either type of probe, always observe correct polarity (GND to GND, pin 1 to pin 1).*

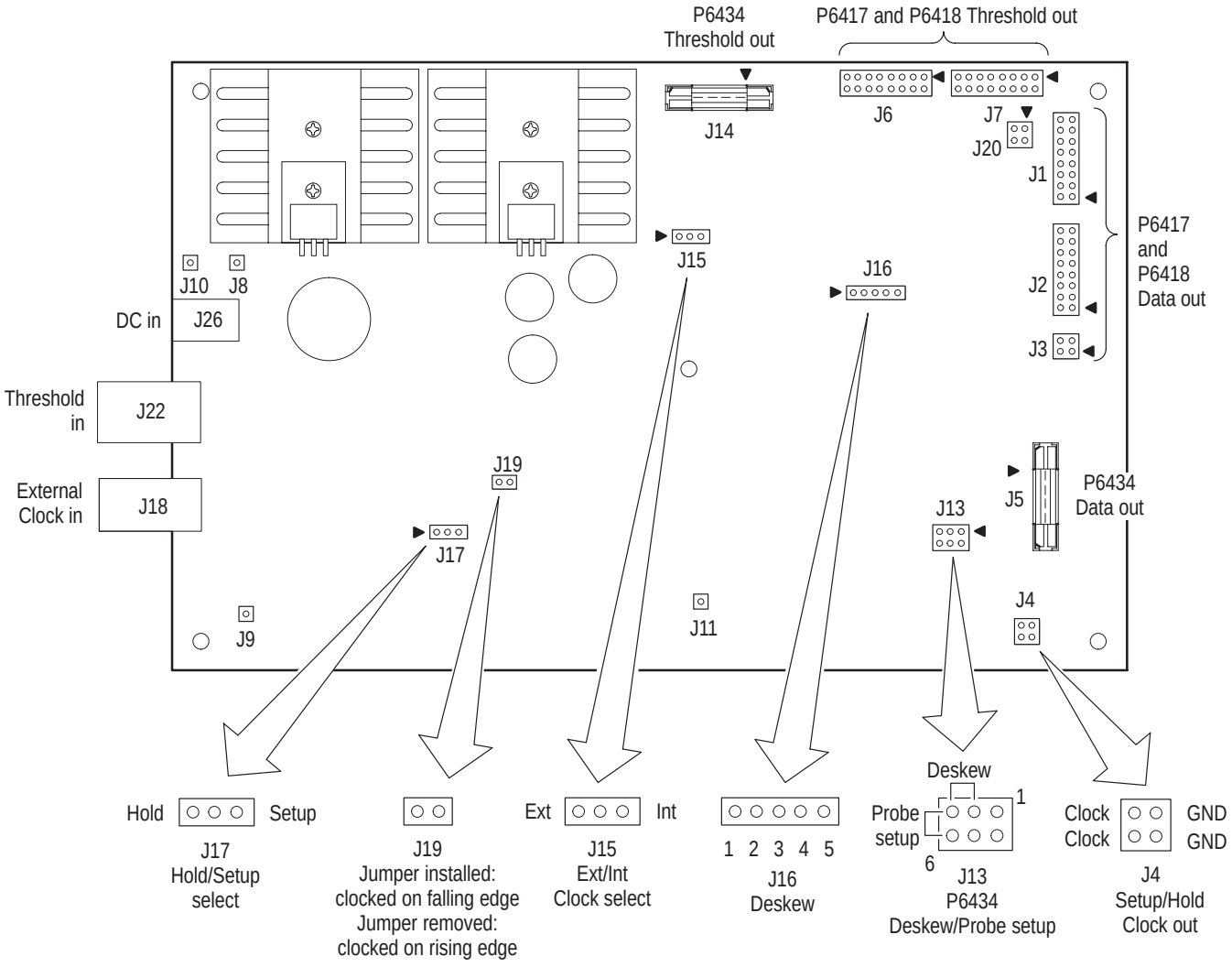

Figure 6–4: Adjustment/verification fixture connections and jumper locations

LA Module Procedure 1: FPV_DC_Threshold

This procedure verifies the DC Threshold Accuracy of the LA Module. This test is performed once and applies to all channels of the module.

SW test name	FPV_DC_Threshold
Equipment required	Adjustment/verification fixture and fixture supply (item 4) Voltage reference (item 26) Precision BNC cable (item 31) Dual banana-to-BNC adapter (item 25) Capacitor, 0.1 µF (item 27)
Prerequisites	Warm-up time: 30 minutes Test equipment connected as shown in Figure 6–5 Diagnostics and SELF_CAL pass

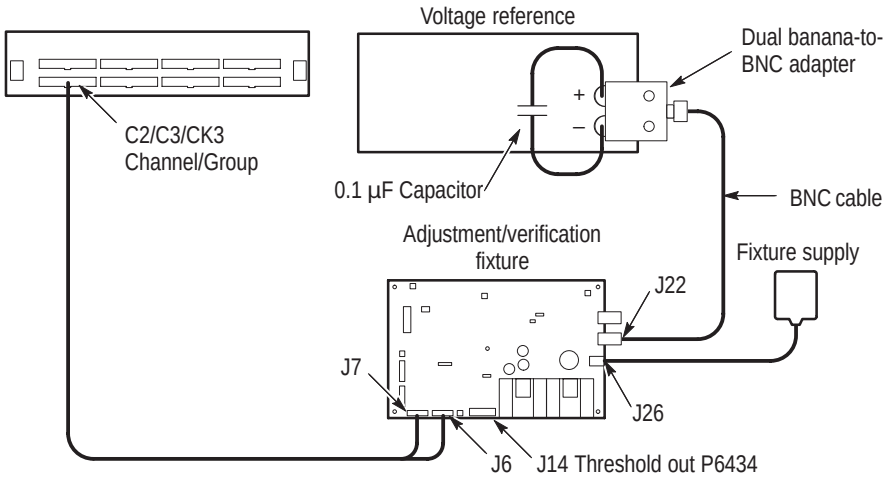

Figure 6–5: FPV_DC_Threshold test setup

1. If the logic analyzer application is running, quit the application. Verify that all of the prerequisites listed previously are met for the procedure.
2. Run the PV/Adjust software as described in *Running the LA and DSO Software* on page 1–12. Run the C:\Tekcats\Tla_la program and then select the correct module type and the PV test option.
3. Follow the on-screen instructions to run each portion of the test for each parameter of the instrument.
4. Verify that all of the tests pass.

LA Module Procedure 2: FPV_Setup_0F

This procedure verifies the setup time of the LA module.

SW test name	FPV_Setup_0F
Equipment required	Adjustment/verification fixture and fixture supply (item 4)
Prerequisites	Warm-up time: 30 minutes Test equipment connected as shown in Figure 6–6 Diagnostics and SELF_CAL pass

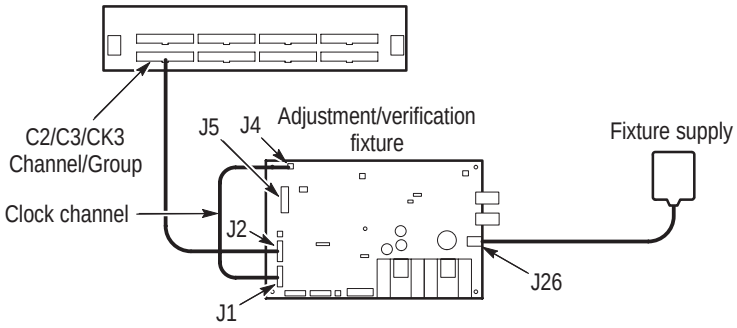

Figure 6–6: Initial FPV_Setup_0F test setup

1. If the logic analyzer application is running, quit the application and verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run each portion of the test for each parameter of the LA module.
3. Verify that all of the tests pass. If a test fails, run the Deskew routine as described on page 6–28, then rerun the test.

LA Module Procedure 3: FPV_Hold_0F

This procedure verifies the hold time of the LA Module.

SW test name	FPV_Hold_0F
Equipment required	Adjustment/verification fixture and fixture supply (item 4)
Prerequisites	Warm-up time: 30 minutes Test equipment connected as shown in Figure 6–7 Diagnostics and SELF_CAL pass

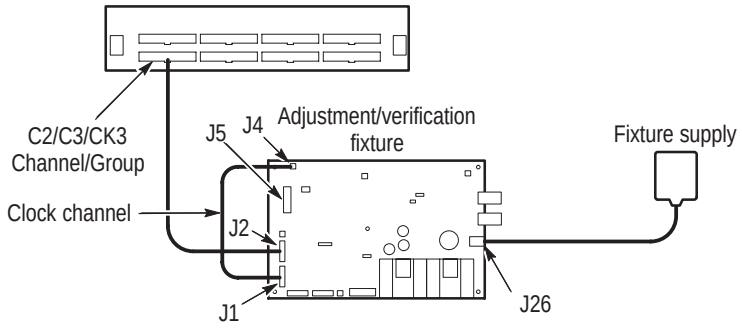

Figure 6–7: Initial FPV_Hold_0F test setup

1. If the logic analyzer application is running, quit the application and verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run each portion of the test for each parameter of the LA module.
3. Verify that all of the tests pass. If a test fails, run the Deskew routine as described on page 6–28, then rerun the test.

LA Module Procedure 4: FPV_Maxsync

This procedure checks the Maximum Synchronous Clock Rate and the Trigger State Sequence Rate of the LA Module. This test is performed once and applies to all channels of the module.

SW test name	FPV_Maxsync
Equipment required	Adjustment/verification fixture and fixture supply (item 4) Sine wave generator (item 33) BNC cable (item 31) Adapter, N-to-BNC (item 29)
Prerequisites	Warm-up time: 30 minutes Test equipment connected as shown in Figure 6–8 Diagnostics and SELF_CAL pass

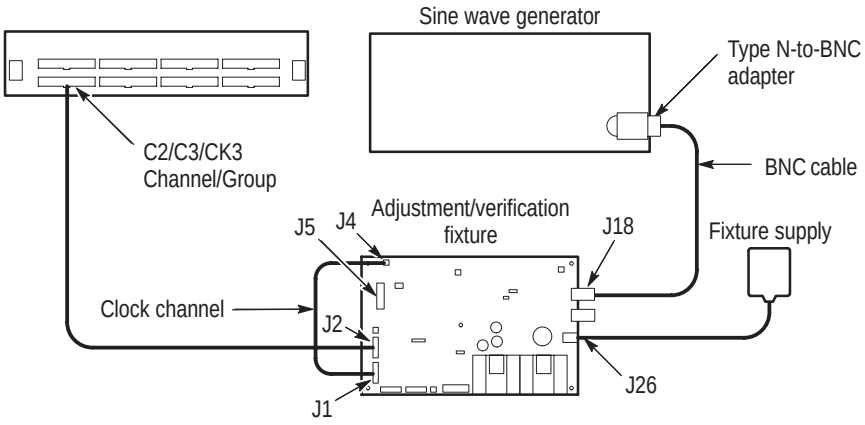

Figure 6–8: FPV_Maxsync test setup

1. If the logic analyzer application is running, quit the application and verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run the test.
3. Verify that all of the tests pass.

Completing the Performance Verification

After completing the performance verification procedures, obtain a copy of the test results and verify that all parameters are within the allowable specifications as listed in the *TLA 700 Series Logic Analyzer User Manual*.

Refer to *Retrieving Test Data from the PV/Adjust Software* on page 1–15 for instructions on obtaining test data.

Logic Analyzer Module Adjustment Procedure

This section contains procedures which use the PV/Adjust software to adjust the TLA7Lx, TLA7Mx, TLA7Nx, TLA7Px, and TLA7Qx logic analyzer modules to within factory specifications. The PV/Adjust software contains instructions and control programs for adjusting the instrument The software describes test equipment connections and settings, selects setup parameters, and loads calibration constants into memory.

These procedures adjust the LA Module for conformance with the warranted characteristics listed in the *Specifications* section of the *TLA 700 Series Logic Analyzer User Manual*.

Adjustments should be done after repair of the module or when performance verification tests have failed.

Prerequisites

These procedures ask for the serial number of the instrument under test. Before installing the modules in the mainframe, record the serial number of the LA module.

You can also access the module serial number through the logic analyzer application. In the application, go to the System menu, select System Properties, and click on the LA instrument tab. You must quit the logic analyzer application before continuing with the PV/Adjust software procedures.

Only trained service technicians should perform this procedure after meeting the following requirements:

- When multiple LA modules of the same model number are installed in the mainframe, the PV/Adjust software will address only the module in the highest-numbered slot. If you are testing a TLA7Q4 module for example, move it to a higher slot number than all of the other TLA7Q4 modules in the mainframe. This avoids unnecessary module warm-up time.
- When adjusting merged modules using the same type of individual modules, the individual modules must be physically separated.
- The TLA system application must not be running.

- The PV/Adjust software must be loaded. Refer to *Software Installation and Removal Instructions* on page 1–8.
- The LA module must be installed in a TLA 700 Series Logic Analyzer.
- The instrument requires a 30-minute warm-up time in a +20° C to +30° C environment before it is adjusted. Adjustments performed before the operating temperature has stabilized may cause errors in performance.

Merged Modules

NOTE. *Only modules with channel widths of 102 or 136 channels can be merged. Two TLA7Lx and TLA7Mx series modules can be merged. Up to three modules can be merged from the TLA7Nx, TLA7Px, and TLA7Qx series modules.*

When adjusting merged modules using the same type of individual modules, for example, three TLA7Q4 modules, the individual modules must be separated before continuing. See the *TLA 700 Series Logic Analyzer User Manual* for instructions on separating merged modules.

NOTE. *The PV/Adjust software runs independent of the logic analyzer application software and does not recognize configuration settings. It is not necessary to unmerge modules through the application software before performing these procedures on merged modules.*

When adjusting merged modules using different types of individual modules, the adjustment procedure can be done on the merged module without physical separation.

NOTE. *After all of the modules have been physically merged, run the self-calibration procedure on the merged modules. To run the self-calibration procedure, go to the System menu, select Calibration and Diagnostics, and then click the Self Calibration tab.*

Using the Software

This section describes how to perform adjustments using the PV/Adjust software.

Performing the Adjustments

There are no manual adjustments for the LA Modules. Instead, the PV/Adjust software adjusts the instrument hardware using external test equipment connections that you provide in response to prompts on the screen.

Upon successful completion of each adjustment, the PV/Adjust software automatically loads the new calibration data into memory.

Adjustment Sequences and Dependencies

The PV/Adjust software allows you to run groups of adjustments, or sequences. A sequence consists of one or more individual adjustments. Normally you will perform a RUN FULL SEQUENCE, which executes each adjustment in the proper order.

The PV/Adjust software also provides instructions for running each adjustment individually. However, you should only perform individual adjustments while troubleshooting.

Adjustment After Repair

You must perform a full adjustment sequence following replacement of any circuit board. Refer to the *TLA7Nx, TLA7Px, and TLA7Qx Logic Analyzer Module Service Manual* for more details.

Test Equipment

In addition to the basic system setup, you will need some of the equipment shown in Table 1–3 on page 1–5 to adjust the LA module.

Each procedure includes a table that calls out the equipment used. Use Table 1–3 to identify required equipment specifications. If you substitute equipment, always choose instruments that meet or exceed the minimum requirements specified.

Adjustment Instructions

This section describes how to perform adjustments using the PV/Adjust software.

Using the PV/Adjust Software

The PV/Adjust software contains instructions for performing the adjustments. The basic steps for completing the procedures follow:

1. Start the program, enter user and product identification information, temperature, and humidity.
2. If you are using P6417 or P6418 probes, label one probe as the Reference Probe, and the other probe as the Probe Under Test.
3. If you are using a P6434 probe, label the probe channel group identified as the pin 38 side as Probe A. Label the probe channel group identified as the pin 1 side as Probe B; refer to Figure 2–9.

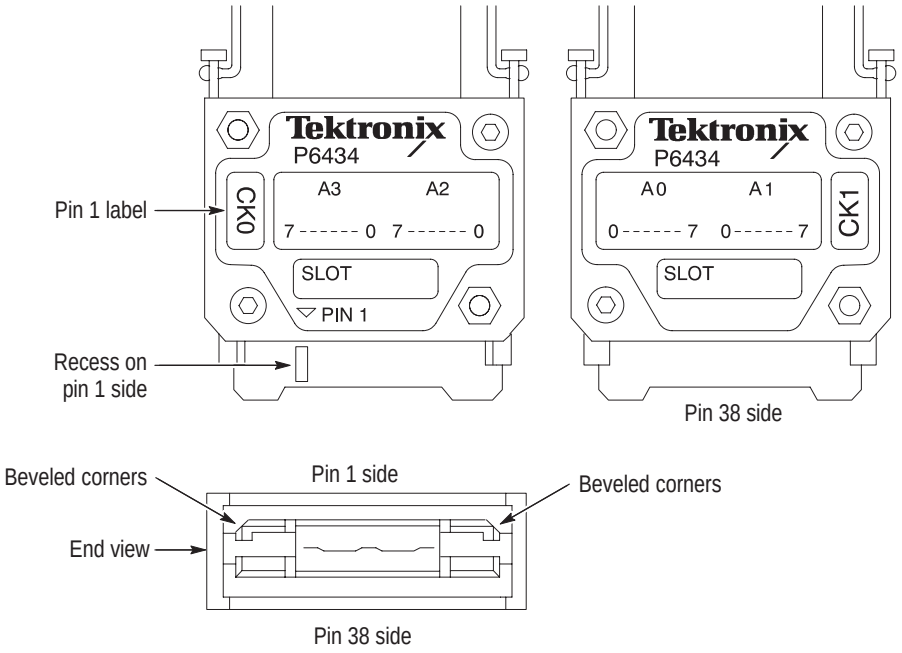

Figure 6–9: P6434 probe detail

4. Select a full adjustment sequence.
5. Connect the test equipment.
6. Set up the test equipment for the output signals described by on-screen instructions and by the connection illustration for each test.

7. Run each adjustment step as instructed by following the on-screen prompts.
8. After completing all the adjustment steps, view the results to confirm that the adjustment was successful.

When a test passes, the software automatically loads new calibration data into memory.

Troubleshooting

If any adjustments fail, use the following steps to troubleshoot the problems:

- Check all test equipment for improper or loose connections.
- Check that all test equipment is powered on and has the proper warm-up time.
- Verify the adjustment/verification fixture LED is lighted and the jumper positions match the on-screen instructions, and the external connections are correct.
- Rerun mainframe or module diagnostics and module self-cal.
- Run the adjustment procedures a second time to verify the failure.
- If the adjustment procedures continue to fail, refer to the *TLA7Nx, TLA7Px, and TLA7Qx Logic Analyzer Module Service Manual* for corrective action.

Tests Performed

The adjustment procedures check and adjust the following parameters of the LA module:

- SELF_CAL, an internal routine in the logic analyzer application software that adjusts acquisition thresholds, internal module signal timing, and merged module signal timing.
- Deskew, an adjustment routine in the PV/Adjust software which time-aligns all channels.

***NOTE**. Do not mix probe types (P6417, P6418, or P6434) when performing the deskew procedure.*

Adjustment Procedures

Refer to the following procedures to identify the initial setup for each adjustment. Then follow the program instructions to complete the adjustments.

Self Calibration

Self calibration is an internal routine that optimizes performance at the current ambient temperature to maximize measurement accuracy. No external equipment or user actions are needed to complete the procedure. The LA module saves data generated by the self calibration in nonvolatile memory. Passing self cal provides a higher level of confidence of module functionality.

NOTE. *Performing the self calibration does not guarantee that all parameters operate within limits. Operation within limits is achieved by performing the adjustment procedures. Verification of operation within limits is accomplished by performing the performance verification procedures.*

When to Perform the Self Calibration. You can run the self calibration at any time during normal operation. To maintain measurement accuracy, perform the self calibration if the following conditions occur:

- After repair and replacement of any circuit board.
- It has been a year since the last self calibration was run
- If you have just merged calibrated LA modules and received an out of calibration on-screen message. You will need to run self calibration on the merged modules.

LA Adjustment Procedure 1: SELF_CAL

Perform the following steps to run the SELF_CAL routine. Before beginning this procedure, be sure that no active signals are applied to the LA module. Self calibration can fail if signals are applied to the probe during the procedure.

Prerequisites	Warm-up time: 30 minutes Power-up diagnostics pass

1. Ensure that the instrument has had a 30-minute warm up before attempting the self calibration, and that the logic analyzer application is running.
2. Disconnect any probes connected to the LA module.
3. Select Calibration and Diagnostics from the System menu.
4. Select the Self Calibration tab page.
5. Select the LA module.
6. Click the Run button to start the self calibration.

   The self calibration takes several minutes to complete, depending on the number of channels in the module. Upon successfully completing the self calibration, the module status changes from Running to Calibrated, and the Date and Time field is set to the present.

LA Adjustment Procedure 2: Deskew

The deskew procedure calibrates and adjusts the timing alignment of the probe data channels and receivers.

Perform the deskew procedure:

- Once a year.
- If you have replaced the LPU board (the probe constants are stored on the LPU board).

This procedure checks and adjusts the time alignment of all channels. There are no manual adjustments.

SW test name	Deskew
Equipment required	Adjustment/verification fixture and fixture supply (item 4) Two P6417 or P6418 Logic Analyzer probes (item 8), OR One P6434 Logic Analyzer probe (item 9)
Prerequisites	Warm-up time: 30 minutes Test equipment connected as shown in Figure 6–10 Merged modules of the same type must be separated and deskewed separately Diagnostics and SELF_CAL pass

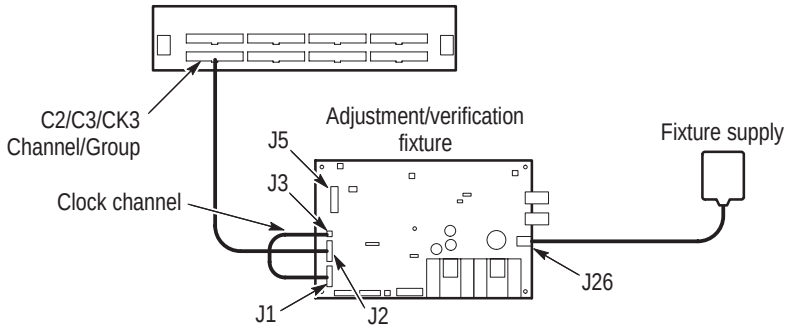

Figure 6–10: Initial deskew test setup

1. If the logic analyzer application is running, quit the application.
2. Verify that all of the prerequisites listed previously are met for the procedure.
3. Load the PV/Adjust software, as described in the *Software Installation and Removal Instructions* on page 1–8.

4. Run the PV/Adjust software, as described in the *Running the LA and DSO Software* on page 1–12. Run the C:\Tekcats\Tla_la program, then select the correct module type and the adjustment option.

***NOTE**. These procedures assume that P6418 or P6417 probes are used. If you have a P6434 probe, use J5, the Data Out connector on the adjustment/verification fixture for performing the deskew test.*

Observe proper polarity: pin 1 to pin 1.

---

5. Follow the on-screen prompts to perform the module deskew adjustment procedure.
6. Verify no failures occur for each test.

If desired, you can print or save the results of the deskew adjustment operation. However, this is not required for calibration. The file will be over-written when the next adjustment or performance verification sequence is run.

Completing the Adjustment Steps

After completing the adjustments, obtain a copy of the test results and verify that all tests passed. Refer to *Retrieving Test Data from the PV/Adjust Software* on page 1–15 for instructions on obtaining test data.

Run the *Performance Verification Procedures* to verify that the all parameters are within the allowable specifications as listed in the *TLA 700 Series Logic Analyzer User Manual*.

Logic Anlayzer Adjustment/Verification Fixture

Adjustment/Verification Fixture Functional Verification

This section contains instructions for performing the functional verification procedure. This procedure provides an easy way to check the basic functionality of the adjustment/verification fixture.

The functional verification procedure consists of the following checks:

- Basic power supply verification
- External clock input circuit verification

This procedure provides a functional check only. If more detailed testing is required, perform the performance verification procedure, which begins on page 7–9, after completing this procedure.

Test Procedure

Use the following procedures to complete the functional verification of the adjustment/verification fixture.

Power Supply

Use the following procedure to verify that the fixture power supply is functional.

1. Plug the fixture power supply included with the adjustment/verification fixture into an appropriate socket and plug the DC connector into J26.
2. The LED adjacent to J26 should light. This indicates the input power supply is functioning properly.

External Clock Input

Use the following procedure to verify the external clock input circuit is dividing the input frequency by two and routing this clock signal to the proper output connectors. This test provides a basic functionality check of the adjustment/verification fixture.

Parameter tested	External clock input
Equipment required	Sine wave generator (item 33) Precision BNC cable (item 31) TDS 784D Oscilloscope (item 6) 1 DSO probe (item 7)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Set the jumper positions as called out in the table. Refer to Figure 7–2 on page 7–12 for jumper locations.

Jumper	Jumper name	Jumper setting
J13	P6434 Setup & Hold/Deskew select	Disconnected
J15	Clock selection	EXT
J16	Deskew	1-2 and 4-5 connected
J17	Setup/hold select	Disconnected
J19	Clock polarity select	Disconnected

2. Connect the sine wave generator to J18, EXT CLK IN, on the adjustment/ verification fixture.
3. Set the generator output to 210 MHz, 1 V p-p.
4. Set up the TDS 784D oscilloscope by pressing Setup, and then press Factory Setup, and then press OK Confirm Factory Init to return the oscilloscope to default conditions.
5. Set up the TDS 784D oscilloscope as listed below.
   - **a.** Set up the CH1 Vertical menu as follows:
     - Coupling DC/50 Ω
     - Fine Scale 200 mV/div
     - Position –3.32 div
   - **b.** Set up the Horizontal menu as follows:
     - Time Base Main
     - Record Length 5000
     - Horizontal Scale Main Scale @ 5 ns/div
   - **c.** Set up the Trigger menu as follows:
     - Source CH1
     - Coupling DC
     - Slope +
     - Level 700 mV
     - Mode Normal

d. Set up the Measure menu as follows:

- Select Measurement for CH1 Frequency
- Gating Off

e. Set up the Cursor menu as follows:

- Function Off

f. Set up the Acquire menu as follows:

- Acquisition Mode Sample
- Repetitive Signal On

6. Using the oscilloscope and the custom probe adapter shown in Figure 7–1 on page 7–10, verify that the output frequency at J1 pin-2 on the adjustment/verification fixture is 105 MHz.

7. Press the Run/Stop button to stop the acquisition.

8. Disconnect the test equipment from the adjustment/verification fixture.

9. This completes the functional verification procedures for the adjustment/verification fixture.

Adjustment/Verification Fixture Certification

The internal system clock and clock output timing are checked for accuracy. The adjustment/verification fixture accuracy is certifiable if these parameters meet specifications.

The procedure is described in the performance verification section, beginning on page 7–9. Record the results in the Calibration Data Report on the following page.

Calibration Data Report

Adjustment/Verification Fixture

Instrument model number: _____

Serial number: _____ Certificate number: _____

Verification performed by: _____ Verification date: _____

Test Data

Characteristic	Specification	Tolerance	Procedure reference	Incoming data	Outgoing data
Internal clock frequency	50.065 MHz	±.01 percent (50.0600 MHz-50.0700 MHz)	Page 7–13, Step 2		
Data Output (Channel-to-Channel Skew)	50 ps	Less than 50 ps	Page 7–15, Step 8		
Setup Clock Output (at R127)	+3.0 ns	±100 ps	Page 7–20, Step 10		
Setup Clock Output (at R321)	+3.0 ns	±100 ps	Page 7–20, Step 12		
Hold Clock Output (at R127)	0.0 ns	±100 ps	Page 7–17, Step 9		
Hold Clock Output (at R321)	0.0 ns	±100 ps	Page 7–18, Step 11		

Tektronix

Adjustment/Verification Fixture Performance Verification

This section contains procedures to verify the accuracy of the adjustment/verification fixture.

Prerequisites

The tests in this section provide a valid confirmation of performance and functionality when the following requirements are met:

- The adjustment/verification fixture must have been operating for a warm-up period of at least 30 minutes, and must be operating at an ambient temperature between +20° C and +30° C.
- The adjustment/verification fixture must have been last adjusted at an ambient temperature between +20° C and +30° C.
- The adjustment/verification fixture must be in an environment within the same limits as for the logic analyzer, described in the *Specifications* section of the *TLA 700 Series Logic Analyzer User Manual*.

These tests should be performed once every two years.

Test Equipment

These procedures use external, traceable signal sources to directly test characteristics that are designated as checked (✓) in the characteristics table in the *Appendix* of this document. You will need some of the equipment shown in Table 1–3 on page 1–5 to complete the performance verification procedures.

Each procedure includes a table that calls out the equipment used; use Table 1–3 for equipment specifications. If you substitute equipment, always choose instruments that meet or exceed the minimum requirements specified.

Tests Performed

Each test verifies one or more parameters.

Table 7–1: Adjustment/verification fixture performance verification tests

Test name	Specification tested
Power supply	V_{DD}
Internal clock frequency[1]	50.065 MHz
Data skew[1]	Less than 50 ps between any 2 channels
Hold time[1]	0.0 ns
Setup time[1]	+3.0 ns

1 **Certifiable parameter**

Custom Probe Tip Adapter

A custom probe tip adapter is used in these procedures to ensure signal integrity when making precise measurements. The primary function of the custom probe tip adapter is to minimize the length of the ground lead of the probe. Build the custom probe tip adapter as shown in Figure 7–1.

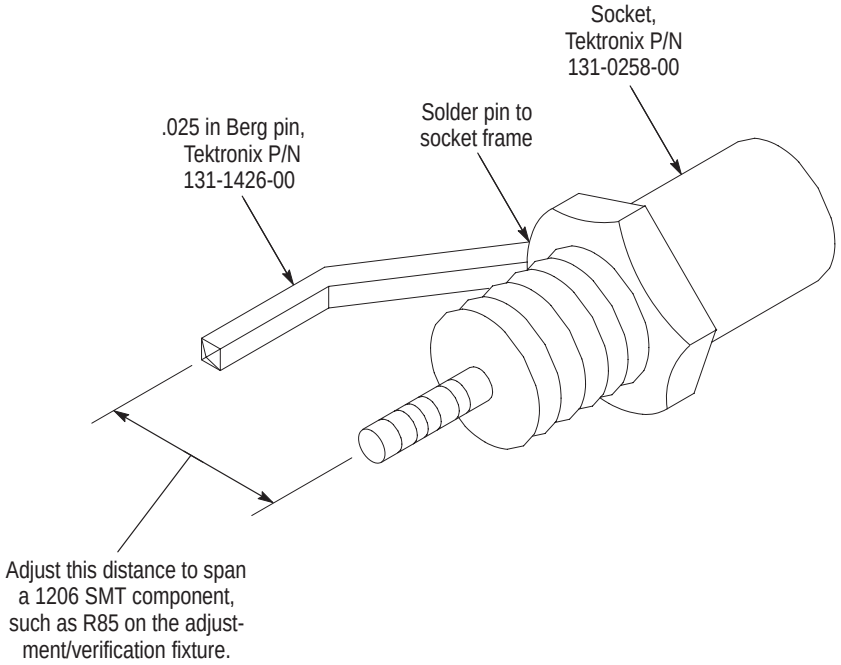

Figure 7–1: Probe tip adapter detail

Test Procedures

Refer to Figure 7–2 on page 7–12 for component and test point locations used in the following procedures. Table 7–2 on page 7–12 describes the functions of the jumpers used on the fixture for verifying the performance of the Tektronix logic analyzers. The jumpers are also used in these procedures.

All procedures must be followed sequentially. If any single step fails or is out of calibration, then upon retest, you must start at the first test and follow this section through from start to finish sequentially.

Power Supply Checks

The following procedures check the DC power supply characteristics.

Parameter tested	Power supply
Equipment required	DMM with test leads (item 24)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Plug the fixture supply into an appropriate AC outlet and connect the DC plug to J26 on the adjustment/verification fixture.
2. Connect the DMM (–) lead to J8 (V_{EE}).
3. Connect the DMM (+) lead to J10 (V_{DD}) and verify a voltage reading of +5.00 V ±100 mV.
4. Leave the (+) lead of the DMM connected to J10 (V_{DD}) and connect the DMM (–) lead to J9 (GND). Verify a voltage reading of +2.00 V ±30 mV.

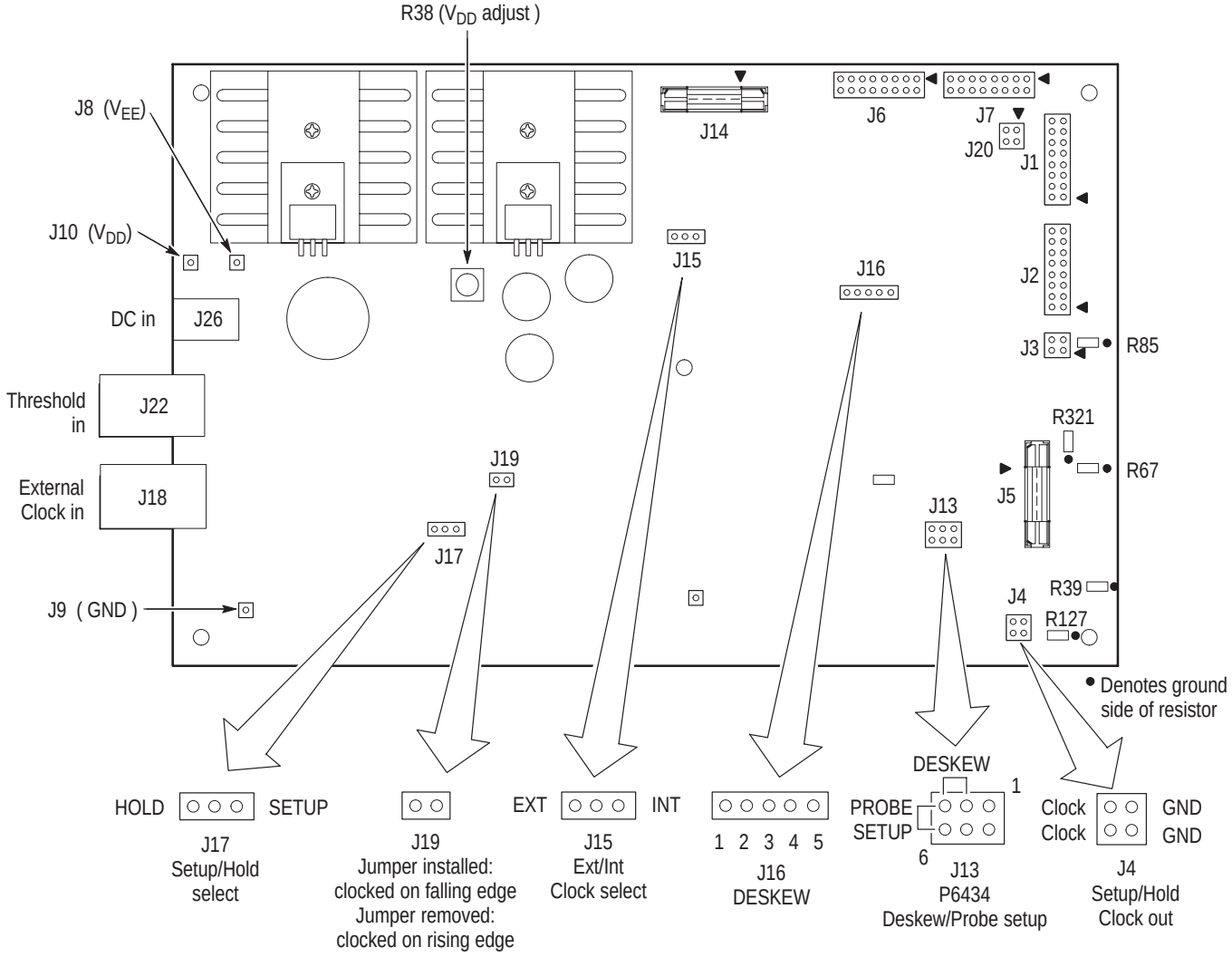

Figure 7–2: Adjustment/verification fixture detail

Table 7–2: Adjustment/verification fixture jumper settings

Jumper	Jumper name	Jumper function
J13	P6434 Deskew/probe setup	Determines whether checking setup/hold or deskew for the P6434 probe (J5)
J15	Clock selection	Determines whether the internal clock (50.065 MHz) or the external clock (J18, BNC) will drive the circuitry
J16	Deskew	Selects between minimum or nominal pulse width
J17	Setup/hold select	Determines whether checking setup time or hold time
J19	Clock polarity select	Selects polarity of the clock for setup and hold testing

Verify Internal Clock Frequency

Use the following procedure to verify the internal clock frequency.

Parameter tested	Internal clock frequency
Equipment required	Frequency counter (item 15)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Set the jumper positions as listed in the table.

Jumper	Jumper name	Jumper setting
J13	P6434 Deskew/probe setup	3-5 connected
J15	Clock selection	INT
J16	Deskew	2-3 and 4-5 connected
J17	Setup/hold select	HOLD
J19	Clock polarity select	Removed

2. Using the frequency counter, measure the oscillator frequency at pin J1-2. The frequency should match what is listed on the Calibration Data report.

3. Record this measurement on the Calibration Data Report.

Verify Data Output Channel-to-Channel Skew

Use the following procedure to verify the channel-to-channel data skew.

Parameter tested	Channel-to-channel data skew
Equipment required	TDS 784D Oscilloscope (item 6) 2 DSO probes (item 7) Custom probe tip adapter (see Figure 7–1, page 7–10)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Set the jumper positions as listed in the following table.

Jumper	Jumper name	Jumper setting
J13	P6434 Deskew/probe setup	3-5 connected
J15	Clock selection	INT
J16	Deskew	2-3 and 4-5 connected
J17	Setup/hold select	HOLD
J19	Clock polarity select	Removed

2. Set up your TDS 784D oscilloscope by pressing Setup, and then press Factory Setup, and then press OK Confirm Factory Init to return the oscilloscope to default conditions.

3. Set up the TDS 784D oscilloscope as listed below.

a. Set up the CH1 and CH2 Vertical menu as follows:

- Coupling DC/50 Ω
- Fine Scale 200 mV/div
- Position –3.00 div CH1
- Position –3.32 div CH2

b. Set up the Horizontal menu as follows:

- Time Base Main
- Record Length 5000
- Horizontal Scale Main Scale @ 2 ns/div

c. Set up the Trigger menu as follows:

- Source CH2
- Coupling DC
- Slope +
- Level 700 mV
- Mode Normal

d. Set up the Measure menu as follows:

- Select Measurement for CH1 Measure
- Gating On

e. Set up the Cursor menu as follows:

- Function V Bars

f. Set up the Acquire menu as follows:

- Acquisition Mode Average 90
- Repetitive Signal On

4. Connect CH2 of the oscilloscope to J4-2 on the adjustment/verification fixture.

5. Select Deskew from the Vertical menu of the oscilloscope.

NOTE. *Observe proper polarity when doing the following steps. See Figure 7–2 on page 7–12 to identify the ground side of the components being measured.*

---

6. Connect the CH1 probe of the oscilloscope to the custom probe tip adapter and measure the signal across R85.

7. Use the large knob at the upper right of the oscilloscope panel to adjust delay until the leading edges of the two waveforms coincide and the displayed value of CH1-CH2 delay is averaged around 0 ±25 ps.

8. Move the CH1 probe to R321, R67, and R39 and press the Run/Stop button to start an acquisition. Verify that the CH1-CH2 delay between any two measurements does not exceed 90 ps.

9. The maximum difference between the three measured values represents the channel-to-channel skew. Record this difference on the Calibration Data Report.

Verify Hold Clock Output Timing

Use the following procedure to verify the hold time.

Parameter tested	Hold time
Equipment required	TDS 784D Oscilloscope (item 6), 2 DSO probes (item 7) Custom probe tip adapter (see Figure 7–1, page 7–10)
Prerequisites	Warm-up time: 30 minutes, adjustment/verification fixture and test equipment

1. Set the jumper positions as listed in the table.

Jumper	Jumper name	Jumper setting
J13	P6434 Deskew/probe setup	1-3 and 5-6 connected
J15	Clock selection	INT
J16	Deskew	1-2 and 4-5 connected
J17	Setup/hold select	HOLD
J19	Clock polarity select	Disconnected

2. Set up your TDS 784D oscilloscope by pressing Setup, and then press Factory Setup, and then press OK Confirm Factory Init to return the oscilloscope to default conditions.

3. Set up the TDS 784D oscilloscope as listed below.

a. Set up the CH1 Vertical menu as follows:

- Coupling DC/50 Ω
- Fine Scale 200 mV/div
- Position –3.00 div CH1
- Position –3.32 div CH2

b. Set up the Horizontal menu as follows:

- Time Base Main
- Record Length 5000
- Horizontal Scale Main Scale @ 2 ns/div

c. Set up the Trigger menu as follows:

- Source CH2
- Coupling DC
- Slope +
- Level 700 mV
- Mode Normal

d. Set up the Measure menu as follows:

- Select Measurement for CH1 Measure
- Gating On

e. Set up the Cursor menu as follows:

- Function V Bars

f. Set up the Acquire menu as follows:

- Acquisition Mode Average 90
- Repetitive Signal On

4. Connect the CH2 probe of the oscilloscope to J1-2 on the adjustment/verification fixture.

5. Select Deskew from the Vertical menu.

NOTE. *Observe proper polarity when performing the following steps.*

See Figure 7–2 on page 7–12 to identify the ground side of the components being measured.

---

6. Connect the CH1 probe of the oscilloscope to the custom probe tip adapter and measure the signal across R67.

7. Begin the acquisition by pressing the Run/Stop button.

8. Use the large knob at the upper right of the panel to adjust delay until the leading edges of the two waveforms coincide and the displayed value of CH1-CH2 delay is averaged around 0.

9. Connect the CH1 probe to R127. Verify the CH1-CH2 delay is averaged around 0 ns ±100 ps.

10. The CH1-CH2 delay represents the hold time at R127. Record the hold time at R127 on the Calibration Data Report.

11. Connect the CH1 probe to R321. Verify the CH1-CH2 delay is averaged around 0 ns ±100 ps.

12. The CH1-CH2 delay represents the hold time at R321. Record the hold time at R321 on the Calibration Data Report.

Verify Setup Clock Output Timing

Use the following procedure to verify the setup time.

Parameter tested	Setup time
Equipment required	TDS 784D Oscilloscope (item 6), 2 DSO probes (item 7) Custom probe tip adapter (see Figure 7–1, page 7–10)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Set the jumper positions as listed in the table.

Jumper	Jumper name	Jumper setting
J13	P6434 Deskew/probe setup	1-3 and 5-6 connected
J15	Clock selection	INT
J16	Deskew	1-2 and 4-5 connected
J17	Setup/hold select	SETUP
J19	Clock polarity select	Disconnected

2. Set up your TDS 784D oscilloscope by pressing Setup, and then press Factory Setup, and then press OK Confirm Factory Init to return the oscilloscope to default conditions.

3. Set up the TDS 784D oscilloscope as listed below.

   a. Set up the CH1 Vertical menu as follows:

   - Coupling DC/50 Ω
   - Fine Scale 200 mV/div
   - Position –3.00 div CH1
   - Position –3.32 div CH2

b. Set up the Horizontal menu as follows:

- Time Base — Main
- Record Length — 5000
- Horizontal Scale — Main Scale @ 2 ns/div

c. Set up the Trigger menu as follows:

- Source — CH2
- Coupling — DC
- Slope — +
- Level — 700 mV
- Mode — Normal

d. Set up the Measure menu as follows:

- Select Measurement for CH1 — Measure
- Gating — On

e. Set up the Cursor menu as follows:

- Function — V Bars

f. Set up the Acquire menu as follows:

- Acquisition Mode — Average 90
- Repetitive Signal — On

4. Connect the CH2 probe of the oscilloscope to J1 pin-2 on the adjustment/verification fixture.

5. Select Deskew from the Vertical menu of the oscilloscope.

NOTE. *Observe proper polarity when doing the following steps. See Figure 7–2 on page 7–12 to identify the ground side of the components being measured.*

6. Connect the CH1 probe of the oscilloscope to the custom probe tip adapter and measure the signal across R67.

7. Press the Run/Stop button to stop the acquisition and read the measurement.

8. Use the large knob at the upper right of the panel to adjust delay until the leading edges of the two waveforms coincide and the displayed value of CH1-CH2 delay is averaged around 0.

9. Set one of the vertical cursors before the leading edge of the CH 2 pulse, and the other cursor after the leading edge of the CH 1 pulse.
10. Connect the CH1 probe to R127. Verify the CH1-CH2 delay is averaged around 3.0 ns ±100 ps.
11. The CH1-CH2 delay represents the setup time at R127. Record the setup time at R127 on the Calibration Data Report.
12. Connect the CH1 probe to R321. Verify the CH1-CH2 delay is averaged around 3.0 ns ±100 ps.
13. The CH1-CH2 delay represents the setup time at R321. Record the setup time at R321 on the Calibration Data Report.

Verify External Clock Input

Use the following procedure to verify the external clock input.

Parameter tested	External Clock Input
Equipment required	Adjustment/verification fixture and power supply DC 508 1 GHz Counter SG 503 Signal Generator Shorting Jumper Connectors, strip of 10 (131–5829–00)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Set the jumper positions as listed in the table.

Jumper	Jumper name	Jumper setting
J13	P6434 Deskew/probe setup	1-3 and 5-6 connected
J15	Clock selection	EXT
J16	Deskew	1-2 and 4-5 connected
J17	Setup/hold select	SETUP
J19	Clock polarity select	Disconnected

2. Using the SG 503, insert a 225 MHz, 1 V_{p-p} signal at J18 EXT CLK IN.
3. Using the DC 508 counter, verify that the data is being output at a 112.5 MHz clocked rate at J1 and J2.

Adjustment/Verification Fixture Adjustment

Adjustment Procedure

The following procedure checks the calibration of the adjustment/verification fixture power supplies by verifying that the measured readings are within specifications.

Equipment Required	Adjustment/verification fixture and power supply (item 4) DMM with test leads (item 24)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

Adjustment/Verification Fixture Adjustment

Equipment Required	Adjustment/verification fixture and power supply (item 4) TDS 784 Digitizing Oscilloscope with Version 4.1 firmware P6245 1 MΩ 10X Oscilloscope probe (2 required) DC 508 1 GHz Counter SG 503 Signal Generator P6101B 1X Probe DMM with test leads (item 24) Shorting Jumper Connectors, strip of 10 (131-5829-00)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Warm up the adjustment/verification fixture and all test equipment.

   a. Plug the +12 V external power supply into fixture and perform the power supply checks and other functional steps while allowing the fixture to warm up for 20 minutes.

   b. Turn on the TDS 784 oscilloscope, SG 503, and DC 508 counter. Allow them to warm up for 20 minutes.

Power Supply Checks

The following procedure checks the DC power supply. Refer to Figure 7–3 for test point locations.

Parameter tested	Power supply
Equipment Required	DMM with test leads (item 24)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

2. Connect the DMM (–) lead to J8 (V_{EE}).
3. Connect the DMM (+) lead to J10 (V_{DD}) and check for a voltage reading of +5 V ± 0.10 V.
4. Connect the DMM negative (–) lead to J9 (GND).
5. Connect the DMM positive (+) lead to J10 (V_{DD}) and adjust R38 for a voltage reading of +2.00 V ±10 mV.

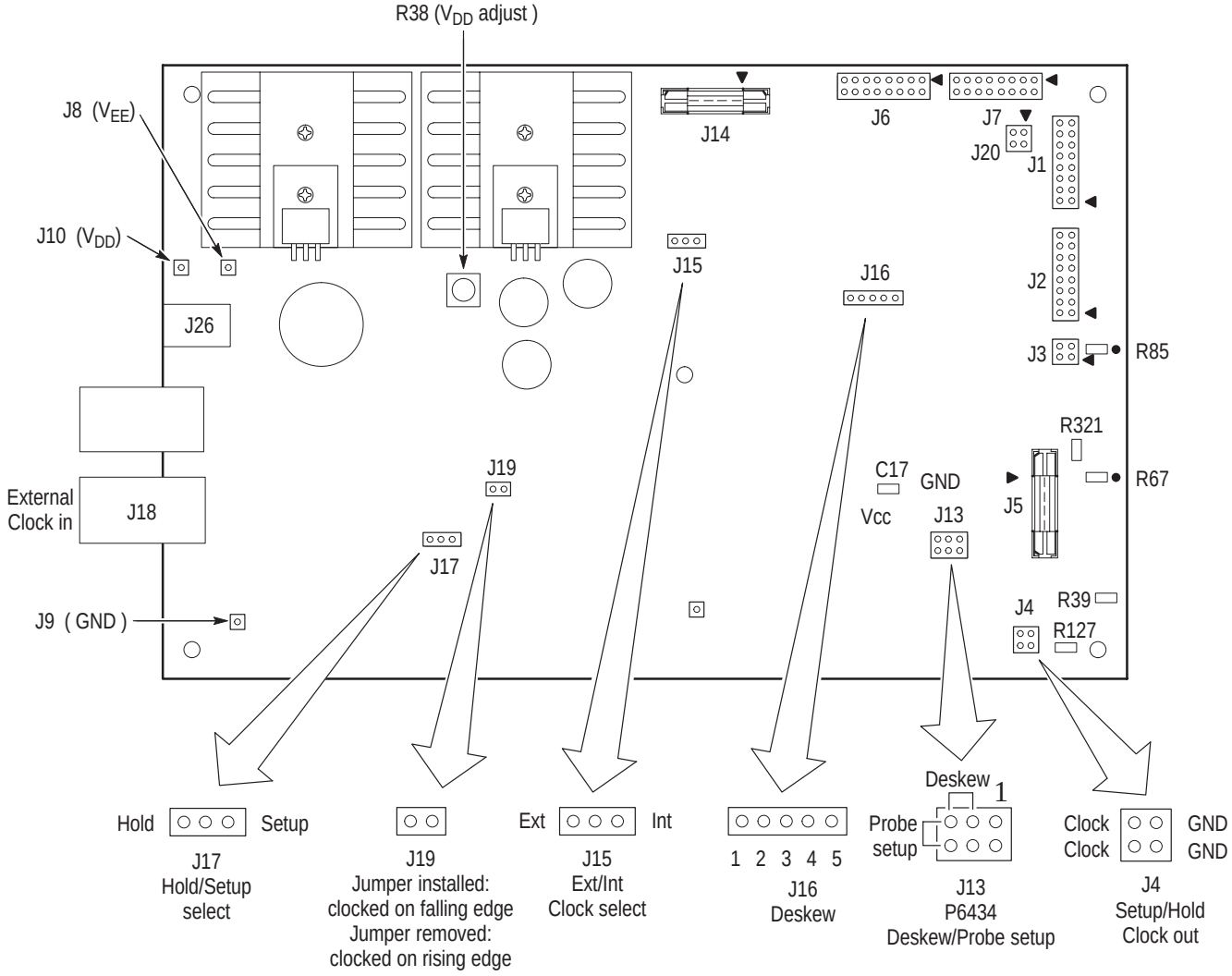

Figure 7–3: Adjustment/verification fixture circuit board layout

Internal Clock Frequency Check

The following procedure checks the internal clock frequency.

Parameter tested	Internal Clock Frequency
Equipment Required	Adjustment/verification fixture and power supply (item 4) DC 508 1 GHz Counter SG 503 Signal Generator Shorting Jumper Connectors, strip of 10 (131-5829-00)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Set up your DC 508 counter as follows:
   - **a.** P6562A Probe: Right input (10 Hz – 100 MHz)
   - **b.** Select Direct Resolution: 10 Hz
   - **c.** 1 M input termination
   - **d.** X1 Attenuation
2. Move one jumper on J16 to DESKEW (pins 2 and 3). Keep the other jumper connected to pins 4 and 5.
3. Using your DC 508 frequency counter, measure the oscillator frequency at J1. It will measure 50.0650 MHz ±0.01% (50.0600 – 50.0700).

Data Pulse Width Adjustment

The following procedure adjusts the data pulse width.

Parameter tested	Data Pulse Width
Equipment Required	Adjustment/verification fixture and power supply (item 4) TDS 784 Digitizing Oscilloscope with Version 4.1 firmware P6245 1 MΩ 10X Oscilloscope probe (2 required) Shorting Jumper Connectors, strip of 10 (131-5829-00)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Set up your TDS 784D oscilloscope by pressing Setup, and then press Factory Setup, and then press OK Confirm Factory Init to return the oscilloscope to default conditions.
2. Set up the TDS 784D oscilloscope as listed below.
   - **a.** Set up the CH1 Vertical menu as follows:
     - Coupling — DC/50 Ω
     - Fine Scale — 200 mV/div
     - Position — –3.32 div
   - **b.** Set up the Horizontal menu as follows:
     - Time Base — Main
     - Record Length — 5000
     - Horizontal Scale — Main Scale @ 1 ns/div
   - **c.** Set up the Trigger menu as follows:
     - Source — CH1
     - Coupling — DC
     - Slope — +
     - Level — 700 mV
     - Mode — Normal
   - **d.** Set up the Measure menu as follows:
     - Select Measurement for CH1 — Measure
     - Gating — Off

e. Set up the Cursor menu as follows:

- Function V Bars

f. Set up the Acquire menu as follows:

- Acquisition Mode Sample
- Repetitive Signal On

3. Move shorting jumpers at J16 to MIN PULSE. Connect the jumpers to pins 1–2, and pins 3–4.

a. Connect the TDS 784 CH1 probe to J2–2. Measure the pulse width using the vertical cursor bars.

b. Using the delay taps on Delay DATA PULSE ADJ, add or subtract the appropriate delay to ensure a 1.9 ns (±50 ps) data pulse width. See Note that follows.

NOTE. *The trace loops on the circuit board add delay according to their length. The longer the loop, the more delay is added to the circuit.*

The loops, from shortest to longest, add approximately 50 ps, 100 ps, 200 ps, 400 ps, and 800 ps respectively.

The length of the jumper wire also adds delay, so care should be used in the length of the jumper wire you add.

It will be necessary to add small loops to the wire jumpers to obtain correct delays and pulse widths on some of the following adjustments.

---

c. Move shorting jumpers at J16 to DESKEW. Connect the jumper to pins 4–5, and 2–3.

d. With the TDS 784 CH1 probe still connected to J2–2, measure the pulse width using the vertical cursor bars.

e. Using the delay taps on Delay DESKEW PULSE ADJ add or subtract the appropriate delay to ensure a 8–10 ns pulse width. See Note following step b.

Data Timing Adjustment

The following procedure is used to adjust the timing.

Parameter tested	Data Timing Adjustment
Equipment Required	Adjustment/verification fixture and power supply (item 4) TDS 784 Digitizing Oscilloscope with Version 4.1 firmware P6245 1 MΩ 10X Oscilloscope probe (2 required) Shorting Jumper Connectors, strip of 10 (131-5829-00)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Install the following jumpers:

Jumper	Jumper name	Jumper setting
J13	P6434 Deskew/probe setup	3-5 connected
J15	Clock selection	INT
J16	Deskew	2-3 and 4-5 connected
J17	Setup/hold select	HOLD
J19	Clock polarity select	Removed

1. Set up your TDS 784D oscilloscope by pressing Setup, and then press Factory Setup, and then press OK Confirm Factory Init to return the oscilloscope to default conditions.

2. Set up the TDS 784D oscilloscope as listed below.

a. Set up the CH1 Vertical menu as follows:

- Coupling DC/50 Ω
- Fine Scale 200 mV/div
- Position –3.32 div

b. Set up the Horizontal menu as follows:

- Time Base Main
- Record Length 5000
- Horizontal Scale Main Scale @ 200 ps/div

c. Set up the Trigger menu as follows:

- Source CH2
- Coupling DC
- Slope +
- Level 700 mV
- Mode Normal

d. Set up the Measure menu as follows:

- Select Measurement for CH1 Measure
- Gating Off

e. Set up the Cursor menu as follows:

- Function V Bars

f. Set up the Acquire menu as follows:

- Acquisition Mode Sample
- Repetitive Signal On

3. Connect the TDS 784 CH2 probe to J4 and trigger on the rising edge of pulse.

4. Connect the TDS 784 CH1 probe to R85 (CLK0) and position the rising-edge on the center graticule.

5. Connect the TDS 784 CH1 probe to R67 (P6434 A) and record the positive delay between R85 and R67 using the vertical cursor bars on the TDS 784.

6. Using the delay taps on Delay CLK1 ADJ, add or subtract the appropriate delay to ensure zero skew (±25 ps) between R85 and R67 (P6434 A). See Note on page 7–26.

7. Connect the TDS 784 CH1 probe to R39 (P6434 B) and record the positive delay between R85 and R39.

8. Using the delay taps on Delay CLK2 ADJ, add or subtract the appropriate delay to ensure zero skew (±25 ps) between R85 and R39 (P6434 B). See Note on page 7–26.

9. Connect the TDS 784 CH1 probe to R321 (P6434 deskew CLK) and record the positive delay between R85 and R321.

10. Using the delay taps on Delay DESKEW CLK ADJ (next to P6434) add or subtract the appropriate delay to ensure zero skew (±25 ps) between R85 and R321 (P6434 deskew CLK). See Note on page 7–26.

Hold Time Adjustment

The following procedure is used to adjust the hold time.

Parameter tested	Hold Time Adjustment
Equipment Required	Adjustment/verification fixture and power supply (item 4) TDS 784 Digitizing Oscilloscope with Version 4.1 firmware P6245 1 MΩ 10X Oscilloscope probe (2 required) Shorting Jumper Connectors, strip of 10 (131-5829-00)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Install the following jumpers:

Jumper	Jumper name	Jumper setting
J13	P6434 Deskew/probe setup	1-3 and 5-6 connected
J15	Clock selection	INT
J16	Deskew	1-2 and 4-5 connected
J17	Setup/hold select	HOLD
J19	Clock polarity select	Removed

1. Set up your TDS 784D oscilloscope by pressing Setup, and then press Factory Setup, and then press OK Confirm Factory Init to return the oscilloscope to default conditions.

2. Set up the TDS 784D oscilloscope as listed below.

a. Set up the CH1 Vertical menu as follows:

- Coupling DC/50 Ω
- Fine Scale 200 mV/div
- Position –3.32 div

b. Set up the Horizontal menu as follows:

- Time Base Main
- Record Length 5000
- Horizontal Scale Main Scale @ 200 ps/div

c. Set up the Trigger menu as follows:

- Source CH2
- Coupling DC
- Slope +
- Level 700 mV
- Mode Normal

d. Set up the Measure menu as follows:

- Select Measurement for CH1 Measure
- Gating Off

e. Set up the Cursor menu as follows:

- Function V Bars

f. Set up the Acquire menu as follows:

- Acquisition Mode Sample
- Repetitive Signal On

3. Connect the TDS 784 CH2 probe to J1 and trigger on the rising edge of the pulse. Connect the TDS 784 CH1 probe to R67 and center the rising edge on the center horizontal graticule.

4. Connect the TDS 784 CH1 probe to R127 and record the difference in timing between R67 and R127 using the vertical cursor bars on the TDS 784.

5. Using the delay taps on delay labeled HOLD ADJ, add or subtract the appropriate delay to ensure zero skew (±25 ps) between R67 and R127 (J4 CLK Out). See Note on page 7–26.

6. Connect the TDS 784 CH1 probe to R321 and record the difference in timing between R67 and R321 using the vertical cursor bars on the TDS 784 (P6434 Setup/Hold timing).

7. Using the delay taps on delay labeled SU/HOLD CLK ADJ. Add or subtract the appropriate delay to ensure zero skew (±25 ps) between R67 and R321 (P6434 deskew CLK Out). See Note on page 7–26.

8. Verify that that J17 has a jumper installed in the HOLD position.

9. Connect the TDS 784 CH1 probe to J2 and center the rising edge on the center horizontal graticule. Trigger on the TDS 784 CH2 probe connected to J1.

10. Connect the TDS 784 CH1 probe to J4 (SU/HOLD CLK OUT) and verify for a 0 skew (±25 ps).

Setup Time Adjustment

The following procedure is used to adjust the setup time.

Parameter tested	Setup Time Adjustment
Equipment Required	Adjustment/verification fixture and power supply (item 4) TDS 784 Digitizing Oscilloscope with Version 4.1 firmware P6245 1 MΩ 10X Oscilloscope probe (2 required) Shorting Jumper Connectors, strip of 10 (131-5829-00)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Install the following jumpers:

Jumper	Jumper name	Jumper setting
J13	P6434 Deskew/probe setup	1-3 and 5-6 connected
J15	Clock selection	INT
J16	Deskew	1-2 and 4-5 connected
J17	Setup/hold select	SETUP
J19	Clock polarity select	Removed

1. Set up your TDS 784D oscilloscope by pressing Setup, and then press Factory Setup, and then press OK Confirm Factory Init to return the oscilloscope to default conditions.

2. Set up the TDS 784D oscilloscope as listed below.

a. Set up the CH1 Vertical menu as follows:

- Coupling DC/50 Ω
- Fine Scale 200 mV/div
- Position –3.32 div

b. Set up the Horizontal menu as follows:

- Time Base Main
- Record Length 5000
- Horizontal Scale Main Scale @ 500 ps/div

c. Set up the Trigger menu as follows:

- Source CH2
- Coupling DC
- Slope +
- Level 700 mV
- Mode Normal

d. Set up the Measure menu as follows:

- Select Measurement for CH1 Measure
- Gating Off

e. Set up the Cursor menu as follows:

- Function V Bars

f. Set up the Acquire menu as follows:

- Acquisition Mode Sample
- Repetitive Signal On

3. Using the delay taps on Delay SETUP ADJ., add or subtract the appropriate delay to ensure a 3.0 ns (±25 ps) timing difference between R67 and R127 (J4 – SU/HOLD CLK OUT). See Note on page 7–26.

4. Install a jumper at J19 and verify that the signal at R127 changes to a Falling Edge.

5. After completing the adjustment/verification fixture adjustment procedure, do the performance verification procedure that starts on page 7–9.

Oscilloscope Module

DSO Module Functional Verification

This section contains instructions for performing the functional verification procedure on the Digital Storage Oscilloscope module. This procedure provides an easy way to check the basic functionality of the DSO module.

If any check within this section fails, refer to the *Troubleshooting* section in the *TLA 7Dx/TLA 7Ex Digitizing Oscilloscope Service Manual* for instructions. Failed tests indicate the instrument needs to be serviced.

The functional verification procedure consists of the following parts:

- Power-on diagnostics
- Extended diagnostics
- Self calibration (Self cal)
- Probe calibration

This procedure provides a functional check only. If more detailed testing is required, perform the performance verification procedure, which begins on page 8–7, after completing this procedure.

Perform these tests whenever you need to gain confidence that the DSO module is operating properly.

Test Equipment

The test equipment used is identified by item numbers described in Table 1–3 on page 1–5. You will need the following equipment to complete the functional verification procedure:

- TLA 700 Series Logic Analyzer mainframe with one DSO module
- One P6243 or P6245 oscilloscope probe, with standard accessories (item 7)
- One DSO probe calibration fixture (item 5)
- One male-male BNC adapter (item 21)

Setup

It is assumed that the DSO module is properly installed and that all accessories are connected. Refer to the *TLA 700 Series Logic Analyzer User Manual* for installation instructions.

Power on the instrument and allow a 30-minute warmup before continuing with any procedures in this section.

Module Self Tests and Power-On Diagnostics

During power-on, the installed modules perform an internal self test to verify basic functionality. No external test equipment is required. The self tests require only a few seconds per module to complete. The front-panel ARM'D and TRIG'D indicators blink during the self test. After testing completes, the front panel indicators have the following states:

- READY — Green (on)
- ACCESSED — off
- ARM'D — off
- TRIG'D — off

Next, the power-on diagnostics are run. If any self tests or power-on diagnostics fail, the instrument will display the Calibration and Diagnostics property sheet.

Extended Diagnostics

Complete the following steps to run the Extended Diagnostics on the DSO module:

1. Go to the System menu and select Calibration and Diagnostics.
2. Click on the Extended Diagnostics tab.

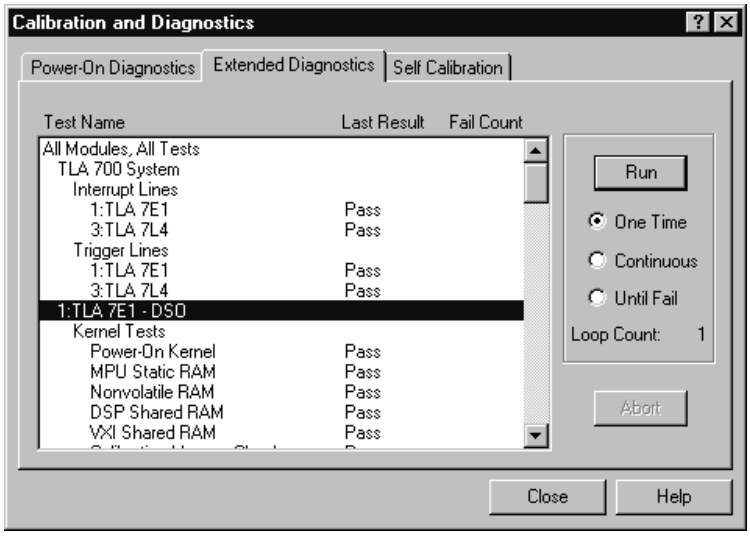

Figure 8–1: Calibration and Diagnostics property sheet

3. Select the top-level test for the module; refer to Figure 8–1.
4. Under the Run button, select One Time.
5. Click the Run button, then click OK to run the extended diagnostics.

   When the instrument runs the extended diagnostics all tests with an Unknown test status will change to either a pass or fail result.
6. When the extended diagnostics are complete, check that all tests for the module have passed.

Self Cal

Self calibration is an internal routine that optimizes performance at the current ambient temperature to maximize measurement accuracy. No external equipment or user actions are needed to complete the procedure. The DSO module saves data generated by the self calibration in nonvolatile memory.

NOTE. *Performing the self calibration does not guarantee that all parameters operate within limits. Operation within limits is checked by performing the performance verification procedures.*

When to Perform Self Calibration

You can run the self calibration at any time during normal operation. To maintain measurement accuracy, perform the self calibration if any of the following conditions occur:

- Operating temperature is not within ±5° C of the temperature when the self calibration was last performed.
- Once a week when the vertical input voltage range of 50 mV/div or less is used.

Running the Self Calibration

Complete the following steps to run the self calibration:

1. Ensure that the instrument has had a 30-minute warmup before attempting the self calibration.
2. Disconnect any probes connected to the DSO module.
3. Go to the System menu and select Calibration and Diagnostics.
4. Select the Self Calibration tab page.
5. Select the DSO module.
6. Click the Run button to start the self calibration.

   The self calibration takes several minutes to complete. Upon successfully completing the self calibration, the module status changes from Running to Calibrated and the Date and Time field is set to the present.

Probe Calibration

You should perform a probe calibration on any active probes that you intend to use with the DSO module. To perform the probe calibration, complete the following steps:

1. Connect an oscilloscope probe to the probe input channel on the DSO module.
2. Connect the DSO probe calibration fixture to the DSO module probe compensation output.
3. Click the Setup button in the DSO module icon.
4. Select the tab page for the input channel.
5. Click the Probe Cal button.
6. Follow the on-screen instructions for completing the probe calibration.

For more information on the probe calibration, refer to the online help.

This completes the functional verification procedure. If all tests passed, the DSO module is ready for use. If any checks failed, refer to the *Troubleshooting* section in the *TLA 7Dx/TLA 7Ex Digitizing Oscilloscope Service Manual* for instructions.

DSO Module Certification

The certification procedures for the DSO module consist of performing the *DSO Module Performance Verification Procedures* and printing the software-generated Calibration Data Report.

DSO Module Performance Verification

This section contains information to verify the performance of the DSO module. Testing is performed using the PV/Adjust software.

The PV/Adjust software contains instructions and control programs for testing each characteristic that is designated as checked (✓) in the *Specifications* section of the *TLA 700 Series Logic Analyzer User Manual*.

As a general rule, these tests should be done once a year.

Prerequisites

These procedures ask for the serial number of the DSO module under test. Before installing the DSO module in the benchtop chassis or portable mainframe, record the serial number of the DSO module.

Alternatively, you can access the module serial number through the logic analyzer application. Go to the System menu, select System Properties, and then click the DSO module tab.

You must quit the logic analyzer application before continuing with the PV/Adjust software procedures.

The tests in this section comprise an extensive, valid confirmation of performance and functionality when the following requirements are met:

- When multiple DSO modules of the same model number are installed in the mainframe, the PV/Adjust software will address only the module in the highest slot number.

  If you are testing a TLA7E1 module, for example, move it to a higher slot number than all other TLA7E1 modules in the mainframe. This method avoids unnecessary module warm-up time.

- The logic analyzer application must not be running, and the PV/Adjust software must be loaded. Refer to *Software Installation and Removal Instructions* on page 1–8.

- The DSO module must be installed in a TLA700 Logic Analyzer, must have been operating for a warm-up period of at least 30 minutes, and must be operating at an ambient temperature between +20° C and +30° C.

- The DSO module must have been last adjusted at an ambient temperature between +20° C and +30° C.

- The TLA700 Logic Analyzer must be in an environment within the limits described in the *Specifications* section of the *TLA 700 Series Logic Analyzer User Manual*.

Using the Software

This section provides a brief overview on using the PV/Adjust software.

When using the PV/Adjust software, you will connect external test equipment to the DSO module in response to prompts on the screen. You will connect the test signals and then instruct the program to continue.

The PV/Adjust software automatically selects the DSO module settings and determines the results of each test. The results of the tests are recorded in a temporary file and are available for printing for certification.

To obtain partial test information you can also run individual tests or selected groups.

***NOTE**. The INTERNAL_CAL (self calibration) test must run successfully before the other tests are performed.*

The remaining tests can be performed in any order.

The PV/Adjust software contains the tests shown in Table 8–1. Each test verifies one or more parameters. All of the tests except INTERNAL_CAL check characteristics that are designated as checked (✓) in the *Specifications* section of the *TLA 700 Series Logic Analyzer User Manual*. By running a full sequence, you will verify the performance of the DSO module.

Table 8–1: DSO PV/Adjust software performance verification tests

Test name	Specification tested
1. INTERNAL_CAL	Runs the internal self cal
2. DC_GAIN_ACCURACY[1]	Accuracy, DC gain
3. OFFSET_ACCURACY[1]	Accuracy, offset
4. ANALOG_BANDWIDTH[1]	Analog bandwidth, DC coupled –50 Ω
5. RANDOM_NOISE[1]	Random noise
6. DELAY_BETWEEN_CHAN[1]	Delay between channels, full bandwidth
7. TIMEBASE_ACCURACY[1]	Accuracy, long term sample rate and delay time

Table 8–1: DSO PV/Adjust software performance verification tests (Cont.)

Test name	Specification tested
8. GLITCH_TRIG_ACC[1]	Accuracy (time) for pulse glitch or pulse width triggering
9. TRIG_MAIN_ACC[1]	Accuracy (DC) for internal and external trigger level, DC coupled
10. TRIG_MAIN_SENS[1]	Sensitivity, edge-type trigger, DC coupled
11. PROBE_COMPENSATION[1]	Probe compensation, output voltage

[1] **Certifiable parameter**

The procedures in this document assume that you will run a full sequence of tests. Each test includes a simple illustration of the test equipment setups and a table summarizing the parameters being verified.

Test Equipment

These procedures use external, traceable signal sources to test characteristics that are designated as checked (✓) in the *Specifications* section of the *TLA 700 Series Logic Analyzer User Manual*.

The test equipment used is identified by item numbers in the table included with each procedure. A full list of test equipment is described in Table 1–3 on page 1–5.

Performance Verification Instructions

You must perform a full performance verification sequence on the DSO module when replacing any circuit board in the module. If the performance verification tests fail, perform the adjustment procedure (see page 8–25), then rerun the performance verification tests.

Using the PV/Adjust Software

The PV/Adjust software contains instructions for performing the performance verification procedure. The basic steps for completing the procedures follow:

1. Start the program and enter user and product identification information.
2. Select a full test sequence.
3. Set up the test equipment for the output signals described by on-screen instructions and by the connection illustration for each test.
4. Run each test as instructed.

***NOTE**. Some tests prompt the you for input on whether to "1:Do Section or 2:Skip Section". It is recommended that you select "Do Section," unless you use the software for troubleshooting.*

5. After completing all the tests, view the test results. Refer to *Retrieving Test Data from the PV/Adjust Software* on page 1–15 for instructions on obtaining test data.

Troubleshooting

If any tests fail, use the following steps to troubleshoot the problems:

1. Check all test equipment for improper or loose connections.
2. Check that all test equipment is powered on and has the proper warm-up time.
3. Run the tests a second time to verify the failure.
4. If tests continue to fail, refer to Table 8–2 to determine the source of the failure and then refer to the *TLA 7Dx/TLA 7Ex Digitizing Oscilloscope Service Manual* for corrective action.

Table 8–2: DSO module fault isolation

Test name	Possible circuit board failure
1. INTERNAL_CAL	A2 Acquisition board
2. DC_GAIN_ACCURACY	A2 Acquisition board
3. OFFSET_ACCURACY	A2 Acquisition board
4. ANALOG_BANDWIDTH	A2 Acquisition board
5. RANDOM_NOISE	A2 Acquisition board
6. DELAY_BETWEEN_CHAN	A2 Acquisition board
7. TIMEBASE_ACCURACY	A2 Acquisition board / Mainframe
8. GLITCH_TRIG_ACC	A2 Acquisition board
9. TRIG_MAIN_ACC	A2 Acquisition board
10. TRIG_MAIN_SENS	A2 Acquisition board
11. PROBE_COMPENSATION	A1 Processor board

Performance Verification Tests

This section describes the individual tests and the test equipment connections. All tests contain a brief table listing the following information:

- Software test name
- A brief list of test equipment
- A list of prerequisites for each test

Most of the tests include a simple test equipment connection diagram (unless there are no changes from the previous test).

DSO Procedure 1: Internal Calibration

This procedure checks the internal self calibration of the DSO module. The INTERNAL_CAL test is the PV/Adjust software equivalent of SELF_CAL.

SW test name	INTERNAL_CAL
Equipment required	None required
Prerequisites	Warm-up time: 30 minutes All probes disconnected Power-up diagnostics pass No previous tests required

1. If the logic analyzer application is running, quit the application.
2. Verify that all of the prerequisites listed previously are met for the procedure.
3. Run the PV/Adjust software as described in *Running the LA and DSO Software* on page 1–12.
4. Select TLA_dig, then select the correct module type and the PV test option.
5. Follow the on-screen instructions to run the test for the DSO module.
6. Verify that this test passes before continuing with any other tests.

DSO Procedure 2: DC Gain Accuracy

This procedure checks the DC gain accuracy of the DSO module.

SW test name	DC_GAIN_ACCURACY
Equipment required	Voltage reference (item 26) Precision BNC cable (item 31) Dual banana-to-BNC adapter (item 25) Capacitor, 0.1 µF[1] (item 27)
Prerequisites	Warm-up time: 30 minutes The logic analyzer application is not running The PV/Adjust software is loaded (see page 1–8) Test equipment connected as shown in Figure 8–2 Power-up diagnostics pass INTERNAL_CAL test passes

1 **Install the 0.1 µF capacitor across the voltage reference output terminals to reduce noise.**

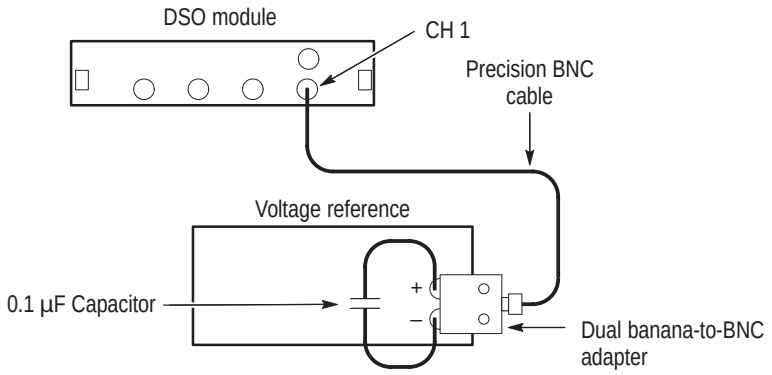

Figure 8–2: Initial setup for the DC gain accuracy test

1. Verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run the test for each channel on the DSO module.
3. After the test begins, make changes to test equipment settings and connections when requested by the on-screen instructions.
4. Verify that all of the tests pass. If a test fails, check the *Troubleshooting* section on page 8–10.

DSO Procedure 3: Offset Accuracy

This procedure checks the offset accuracy of the DSO module.

SW test name	OFFSET_ACCURACY
Equipment required	No change from the DC Gain Accuracy test
Prerequisites	Warm-up time: 30 minutes The logic analyzer application is not running The PV/Adjust software is loaded (see page 1–8) Test equipment connected as shown in Figure 8–2 Power-up diagnostics pass INTERNAL_CAL test passes

1. Verify that all of the prerequisites listed previously are met for the procedure.

WARNING. *These procedures use voltage levels that step through ±99.90 volts. Use caution when using voltages approaching this magnitude.*

2. Follow the on-screen instructions to run the test for each channel on the DSO module.
3. After the test begins, make changes to test equipment settings and connections when requested by the on-screen instructions.
4. Verify that all of the tests pass. If a test fails, check the *Troubleshooting* section on page 8–10.

DSO Procedure 4: Analog Bandwidth

This procedure checks the analog bandwidth, DC coupled specification of the DSO module.

SW test name	ANALOG_BANDWIDTH
Equipment required	Sine wave generator[1] (item 33) Precision BNC cable (item 31) Type N-to-BNC adapter (item 29)
Prerequisites	Warm-up time: 30 minutes The logic analyzer application is not running The PV/Adjust software is loaded (see page 1–8) Test equipment connected as shown in Figure 8–3[2] Power-up diagnostics pass INTERNAL_CAL test passes

1 **The output frequency of the sine wave generator must maintain a constant output amplitude within 0.35 dB of the reference frequency (10 MHz) through the bandwidth calibration frequency range (1005 MHz).**

2 **If you require a power meter to maintain a constant output amplitude use the equipment setup as shown in Figure 8–4.**

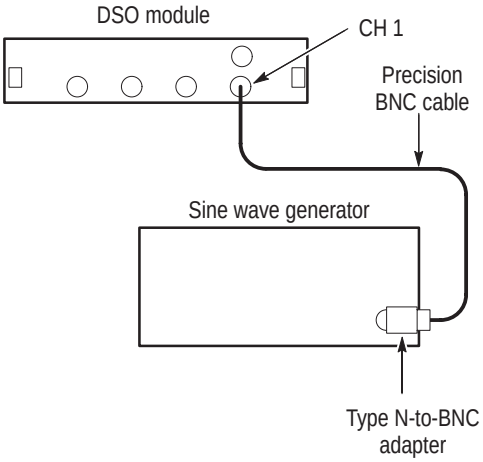

Figure 8–3: Initial setup for the analog bandwidth test

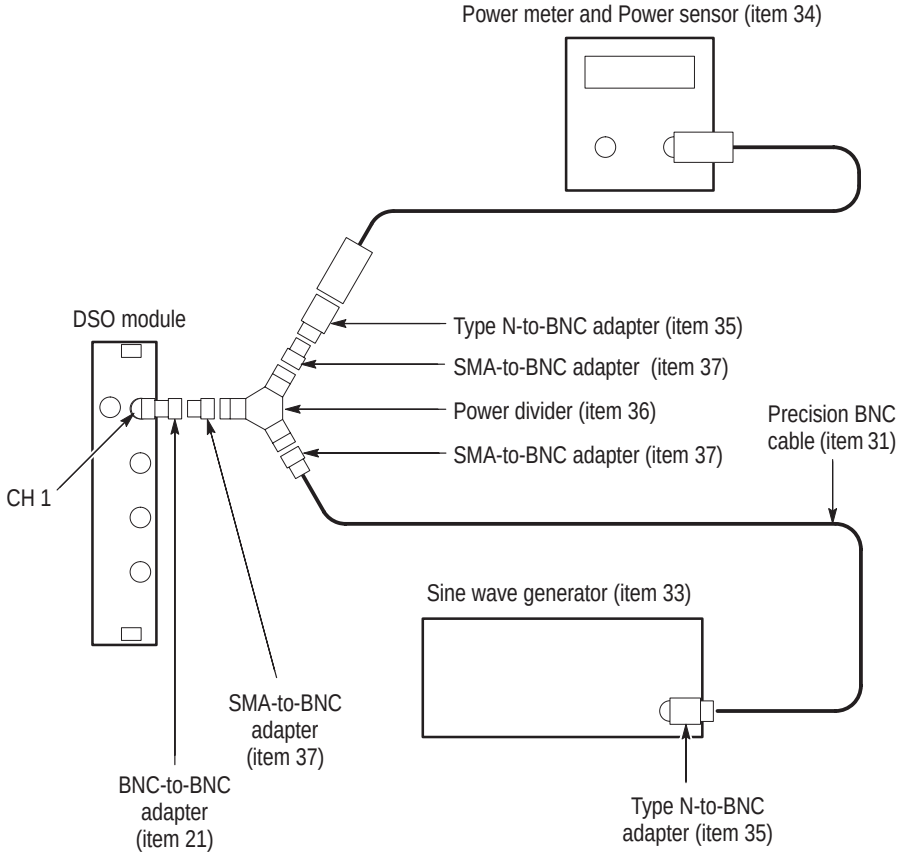

Figure 8–4: Using a power meter to monitor the amplitude of the sine wave generator during the analog bandwidth test

1. Verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run the test for each channel on the DSO module.
3. Verify that all of the tests pass. If a test fails, check the *Troubleshooting* section on page 8–10.

DSO Procedure 5: Random Noise

This procedure checks the random noise specification of the DSO module.

SW test name	RANDOM_NOISE
Equipment required	No external test equipment required
Prerequisites	Warm-up time: 30 minutes The logic analyzer application is not running The PV/Adjust software is loaded (see page 1–8) Power-up diagnostics pass INTERNAL_CAL test passes

1. Verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run the test for the DSO module.
3. Verify that all of the tests pass. If a test fails, check the *Troubleshooting* section on page 8–10.

DSO Procedure 6: Delay Between Channels

This procedure checks the delay between channels for the full bandwidth of the DSO module.

SW test name	DELAY_BETWEEN_CHAN
Equipment required	Sine wave generator (item 33) Precision BNC cable (item 31) Dual input BNC cable[1] (item 28) Type N-to-BNC adapter (item 29)
Prerequisites	Warm-up time: 30 minutes The logic analyzer application is not running The PV/Adjust software is loaded (see page 1–8) Test equipment connected as shown in Figure 8–5 Power-up diagnostics pass INTERNAL_CAL test passes

1 **Use the dual input cable or a set of matched cables when running this test. If you use unmatched coaxial cables, the test may fail or may be miscalibrated due to an electrical mismatch between the cables.**

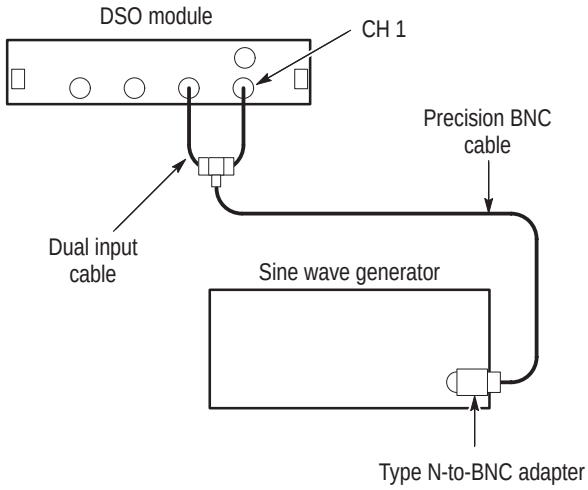

Figure 8–5: Initial setup for the delay between channels test

1. Verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run the test for the DSO module.
3. Verify that all of the tests pass. If a test fails, check the *Troubleshooting* section on page 8–10.

DSO Procedure 7: Timebase Accuracy

This procedure checks the long-term sample rate and delay time accuracy of the DSO module.

SW test name	TIMEBASE_ACCURACY
Equipment required	Sine wave generator (item 33) Precision BNC cable (item 31) Type N-to-BNC adapter (item 29)
Prerequisites	Warm-up time: 30 minutes The logic analyzer application is not running The PV/Adjust software is loaded (see page 1–8) Test equipment connected as shown in Figure 8–6 Power-up diagnostics pass INTERNAL_CAL test passes

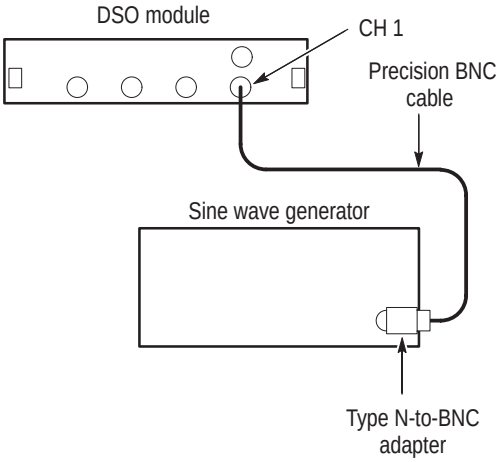

Figure 8–6: Initial setup for the timebase accuracy test

1. Verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run the test for the DSO module.
3. Verify that all of the tests pass. If a test fails, check the *Troubleshooting* section on page 8–10.

DSO Procedure 8: Glitch Trigger Accuracy

This procedure checks the time accuracy for the pulse glitch or for the pulse width triggering of the DSO module.

SW test name	GLITCH_TRIG_ACC
Equipment required	No change from the previous test (Timebase Accuracy)
Prerequisites	Warm-up time: 30 minutes The logic analyzer application is not running The PV/Adjust software is loaded (see page 1–8) Test equipment connected as shown in Figure 8–6 Power-up diagnostics pass INTERNAL_CAL test passes

1. Verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run the test for the DSO module.
3. Verify that all of the tests pass. If a test fails, check the *Troubleshooting* section on page 8–10.

DSO Procedure 9: Main Trigger Accuracy

This procedure checks the DC accuracy for the internal and external trigger level (DC coupled) of the DSO module.

SW test name	TRIG_MAIN_ACC
Equipment required	Function generator (item 32) Precision BNC cable (item 31)
Prerequisites	Warm-up time: 30 minutes The logic analyzer application is not running The PV/Adjust software is loaded (see page 1–8) Test equipment connected as shown in Figure 8–7 Power-up diagnostics pass INTERNAL_CAL test passes

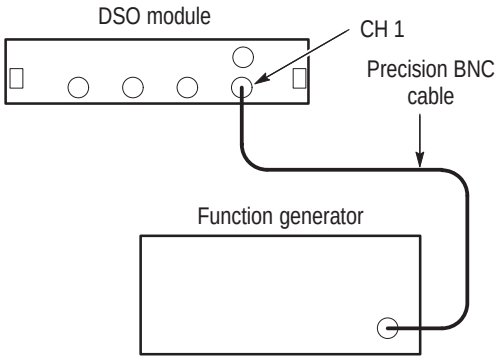

Figure 8–7: Initial setup for the main trigger accuracy test

1. Verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run the test for the DSO module.
3. Verify that all of the tests pass. If a test fails, check the *Troubleshooting* section on page 8–10.

DSO Procedure 10: Main Trigger Sensitivity

This procedure checks the sensitivity of the edge-type trigger (DC coupled) of the DSO module.

SW test name	TRIG_MAIN_SENS
Equipment required	Sine wave generator (item 33) Precision BNC cable (item 31) Type N-to-BNC adapter (item 29)
Prerequisites	Warm-up time: 30 minutes The logic analyzer application is not running The PV/Adjust software is loaded (see page 1–8) Test equipment connected as shown in Figure 8–8 Power-up diagnostics pass INTERNAL_CAL test passes

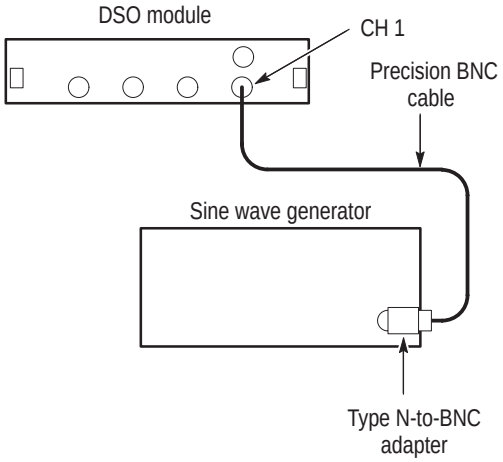

Figure 8–8: Initial setup for the main trigger sensitivity test

1. Verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run the test for the DSO module.
3. Verify that all of the tests pass. If a test fails, check the *Troubleshooting* section on page 8–10.

DSO Procedure 11: Probe Compensation

This procedure checks the probe compensation output voltage of the DSO module.

SW test name	TRIG_MAIN_SENS
Equipment required	Digital multimeter (item 24) Precision BNC cable (item 31) Dual banana-to-BNC adapter (item 25)
Prerequisites	Warm-up time: 30 minutes The logic analyzer application is not running The PV/Adjust software is loaded (see page 1–8) Test equipment connected as shown in Figure 8–9 Power-up diagnostics pass INTERNAL_CAL test passes

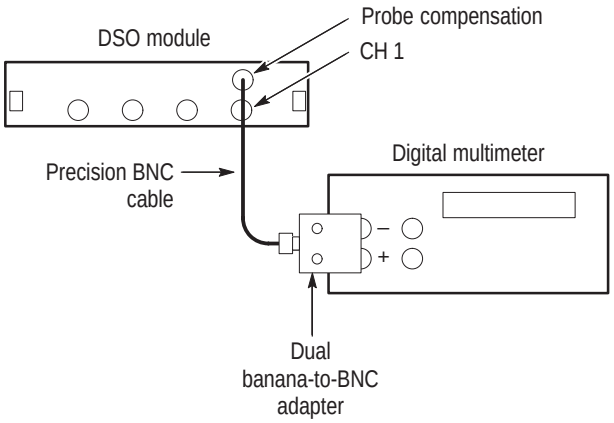

Figure 8–9: Initial setup for the probe compensation test

1. Verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run the test for the DSO module.
3. Verify that all of the tests pass. If a test fails, check the *Troubleshooting* section on page 8–10.

Completing the Performance Verification

After completing the performance verification procedures, obtain a copy of the test results and verify that all parameters are within the allowable specifications as listed in the *TLA 700 Series Logic Analyzer User Manual*.

Refer to *Retrieving Test Data from the PV/Adjust Software* on page 1–15 for instructions on obtaining test data.

DSO Module Adjustment

This section contains information needed to adjust the DSO module. Adjustments are performed using the PV/Adjust software. The PV/Adjust software contains instructions and control programs for adjusting the DSO module.

The software describes test equipment connections and settings, selects DSO module setup parameters, and loads calibration constants into the DSO module memory.

These procedures adjust the DSO module for conformance with the warranted characteristics listed in the *Specifications* chapter of the *TLA 700 Series Logic Analyzer User Manual*.

These adjustments should be done whenever the DSO module fails the performance verification procedure.

Prerequisites

These procedures ask for the serial number of the DSO module under test. Before installing the DSO module in the benchtop chassis or portable mainframe, record the serial number of the DSO module.

Alternatively, you can access the module serial number through the logic analyzer application. In the logic analyzer application, go to the System menu, select System Properties, and then click the DSO module tab. You must quit the logic analyzer application before continuing with the PV/Adjust software procedures.

Only trained service technicians should perform this procedure after meeting the following requirements:

- When multiple DSO modules of the same model number are installed in the mainframe, the PV/Adjust software will address only the module in the highest slot number.

  If you are testing a TLA7E1 module for example, move it to a higher slot number than all other TLA7E1 modules in the mainframe. This method avoids unnecessary module warm-up time.

- The logic analyzer application must not be running.
- The PV/Adjust software must be loaded. Refer to *Software Installation and Removal Instructions* on page 1–8.
- The DSO module requires a 30-minute warm-up time in a +20° C to +30° C environment before it is adjusted. Adjustments performed before the operating temperature has stabilized may cause errors in performance.

Using the Software

This section describes how to perform adjustments using the PV/Adjust software.

Performing the Adjustments

There are no manual adjustments for the DSO module. The PV/Adjust software adjusts the instrument hardware using external test equipment connection you provide in response to prompts on the screen.

Upon successful completion of each adjustment, the PV/Adjust software automatically loads the new calibration data into the DSO module memory.

Adjustment Sequences and Dependencies

The PV/Adjust software allows you to run groups of adjustments, or sequences. A sequence consists of one or more individual adjustments. Normally you will perform a RUN FULL SEQUENCE, which executes each adjustment in the proper order. The PV/Adjust software also provides instructions for running each adjustment individually. However, you should only perform individual adjustments while troubleshooting the DSO module.

Some adjustments depend on successful prior completion of other adjustments. For example, all the tests associated with the Base Calibration must pass before any other adjustments can be successfully completed.

Table 8–3 lists the tests and dependencies for each adjustment.

Table 8–3: DSO Adjustments and dependencies

Adjustment procedure	Tests	Prior completion requirements
1. Base Calibration Adjustment[1]	EXTERNAL_CAL INTERNAL_CAL	None
2. Frequency Response Adjustment (TLA 7E1 and TLA 7E2 only)	BANDWIDTH_CAL	Base Calibration
3. Pulse Trigger Adjustment[2]	GLITCH_TRIG_CAL PNP_LATENCY_CAL	Base Calibration
4. Setup and Hold Adjustment	SETUP_HOLD	Base Calibration Pulse Trigger Adjustment
5. Channel to Channel Skew Adjustment	CHAN_SKEW_CAL	Base Calibration
6. Probe Compensation Adjustment	PROBE_COMP_CAL	None

1 **You must complete the EXTERNAL_CAL test before running the INTERNAL_CAL test.**

2 **You must complete the GLITCH_TRIG_CAL test before running the PNP_LATENCY_CAL test.**

Adjustment After Repair

You must perform a full performance verification sequence following replacement of any circuit board in the DSO module. If the performance verification tests fail, then perform the adjustment procedure.

Refer to the maintenance section of the *TLA 7Dx/TLA 7Ex Digitizing Oscilloscope Service Manual* for more details.

Test Equipment

Table 1–3 on page 1–5 lists the test equipment required to adjust the DSO module. Item numbers under each test in these procedures correspond to the test equipment listed in the Table 1–3.

Adjustment Instructions

This section describes how to perform adjustments using the PV/Adjust software.

Using the PV/Adjust Software

The PV/Adjust software contains instructions for performing the adjustments. The basic steps for completing the procedures follow:

1. Start the program and enter user and product identification information.
2. Select a full adjustment sequence.
3. Connect the test equipment.
4. Run each adjustment step as instructed.
5. After completing all the adjustment steps, view the test results to confirm that the adjustment was successful.

When a test passes, the software automatically loads new calibration data into the DSO module memory.

NOTE. *Use the dual input cable or a set of matched cables (for electrical length) when running the CHAN_SKEW_CAL test.*

If you use unmatched separate coaxial cables, the adjustment may fail or may be miscalibrated due to an electrical mismatch between the cables.

Troubleshooting

If any adjustments fail, use the following steps to troubleshoot the problems:

1. Check all test equipment for improper or loose connections.
2. Check that all test equipment is powered on and has the proper warm-up time.
3. Run the adjustment procedures a second time to verify the failure.
4. If the adjustment procedures continue to fail, refer to Table 8–4 to determine the source of the failure and then refer to the *TLA 7Dx/TLA 7Ex Digitizing Oscilloscope Service Manual* for corrective action.

Table 8–4: Fault isolation

Adjustment procedure	Tests	Possible circuit board failure
1. Base calibration adjustment	EXTERNAL_CAL INTERNAL_CAL	A2 Acquisition board
2. Frequency response adjustment	BANDWIDTH_CAL	A2 Acquisition board
3. Pulse trigger adjustment	GLITCH_TRIG_CAL PNP_LATENCY_CAL	A2 Acquisition board
4. Setup and hold adjustment	SETUP_HOLD	A2 Acquisition board
5. Channel to channel skew adjustment	CHAN_SKEW_CAL	A2 Acquisition board
6. Probe compensation adjustment	PROBE_COMP_CAL	A1 Processor board

Adjustment Procedures

Each of the following adjustment procedures corresponds to one or more adjustment control programs in the PV/Adjust software. Refer to the following procedures to identify the initial setup for each test. Then follow the program instructions to complete the tests.

DSO Procedure 1: Base Calibration

This procedure performs an internal and external calibration on the DSO module. The INTERNAL_CAL test is the PV/Adjust software equivalent of SELF_CAL.

SW test names	EXTERNAL_CAL, INTERNAL_CAL
Equipment required	Voltage reference (item 26) Precision BNC cable (item 31) Dual banana-to-BNC adapter (item 25) Capacitor, 0.1 µF[1] (item 27)
Prerequisites	Warm-up time: 30 minutes Test equipment connected as shown in Figure 8–10 Power-up diagnostics pass No previous tests required

1 **Install the 0.1 µF capacitor across the voltage reference output terminals to reduce noise.**

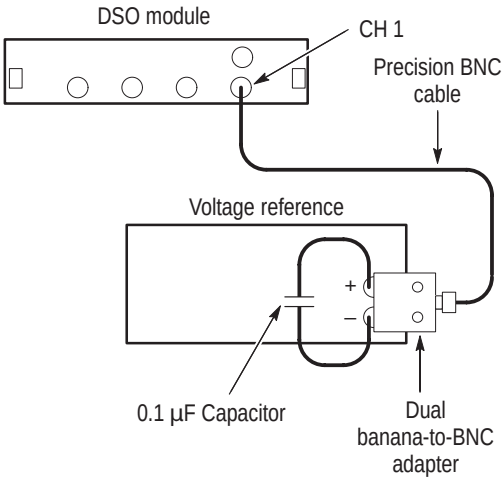

Figure 8–10: Initial setup for the base calibration adjustment

1. If the logic analyzer application is running, quit the application.
2. Load the PV/Adjust software as described in the *Software Installation and Removal Instructions* on page 1–8.
3. Verify that all of the prerequisites listed previously are met for the procedure.
4. Run the PV/Adjust software as described in *Running the LA and DSO Software* on page 1–12. Select TLA_dig, then select the correct module type and the ADJ test option.
5. Follow the on-screen instructions to run the EXTERNAL_CAL test for the DSO module.
6. Verify that the EXTERNAL_CAL test passes before disconnecting the test equipment and performing the INTERNAL_CAL test.
7. Verify that these tests pass before continuing with any other tests.

DSO Procedure 2: Frequency Response Adjustment

This procedure adjusts the frequency response of the TLA 7E1 and the TLA 7E2 DSO modules.

SW test names	BANDWIDTH_CAL
Equipment required	Sine wave generator[1] (item 33) Precision BNC cable (item 31) Type N-to-BNC adapter (item 35)
Prerequisites	Warm-up time: 30 minutes The logic analyzer application is not running Test equipment connected as shown in Figure 8–11[2] Power-up diagnostics pass Base Calibration completed

1 **The output frequency of the sine wave generator must maintain a constant output amplitude within 0.35 dB of the reference frequency (10 MHz) through the bandwidth calibration frequency range (1005 MHz).**

2 **If you require a power meter to maintain a constant output amplitude use the equipment setup as shown in Figure 8–12.**

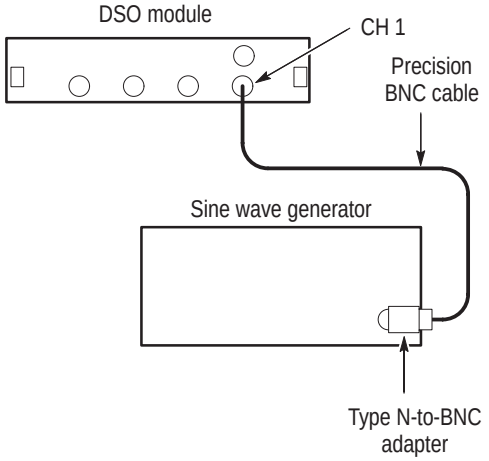

Figure 8–11: Initial setup for the frequency response adjustment

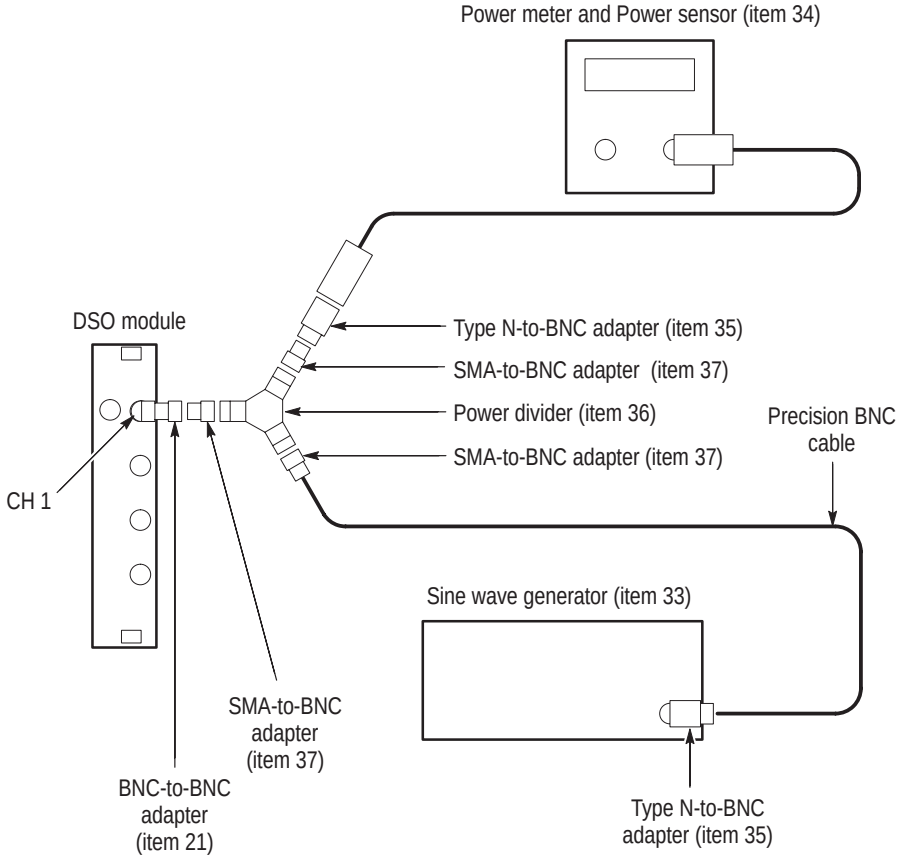

Figure 8–12: Using a power meter to monitor the amplitude of the sine wave generator during the frequency response adjustment

1. Verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run all of the tests for the DSO module.

NOTE. *All of the tests that are listed must be run. There are no optional tests.*

3. Verify no failures occur for each test. If a test continues to fail, check the *Troubleshooting* section on page 8–29.

DSO Procedure 3: Pulse Trigger Adjustment

This procedure adjusts the pulse trigger of the DSO module.

SW test names	GLITCH_TRIG_CAL, PNP_LATENCY_CAL
Equipment required	No changes from the previous test (Frequency Response Adjustment), unless power meter was used
Prerequisites	Warm-up time: 30 minutes The logic analyzer application is not running Test equipment connected as shown in Figure 8–11 Power-up diagnostics pass Base Calibration completed

1. Verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run all of the tests for the DSO module.

NOTE. *All of the tests that are listed must be run. There are no optional tests.*

3. Verify no failures occur for each test. If a test continues to fail, check the *Troubleshooting* section on page 8–29.

DSO Procedure 4: Setup and Hold Adjustment

This procedure adjusts the setup and hold parameters of the DSO module.

SW test names	SETUP_HOLD_CAL
Equipment required	No change from previous test
Prerequisites	Warm-up time: 30 minutes The logic analyzer application is not running Test equipment connected as shown in Figure 8–11 Power-up diagnostics pass Base Calibration and Pulse Trigger adjustment completed

1. Verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run the test for the DSO module.
3. Verify no failures occur for each test. If a test continues to fail, check the *Troubleshooting* section on page 8–29.

DSO Procedure 5: Channel-to-Channel Skew Adjustment

This procedure adjusts the channel-to-channel skew parameters of the DSO module.

SW test names	CHAN_SKEW_CAL
Equipment required	Sine wave generator (item 33) Precision BNC cable (item 31) Dual input BNC cable[1] (item 28) Type N-to-BNC adapter (item 29)
Prerequisites	Warm-up time: 30 minutes The logic analyzer application is not running Test equipment connected as shown in Figure 8–13 Power-up diagnostics pass Base Calibration completed

1 **Use the dual input cable or a set of matched cables when running this test. If you use unmatched coaxial cables, the test may fail or may be mis-calibrated due to an electrical mismatch between the cables.**

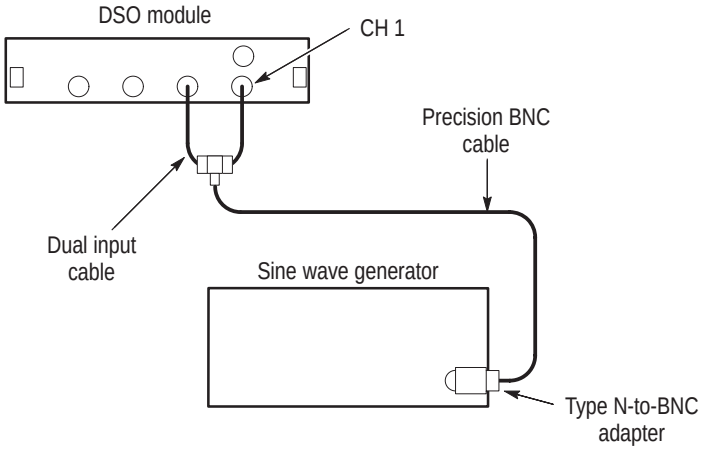

Figure 8–13: Initial setup for the channel-to-channel skew adjustment

1. Verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run the test for the DSO module.
3. Verify no failures occur for each test. If a test continues to fail, check the *Troubleshooting* section on page 8–29.

DSO Procedure 6: Probe Compensation Adjustment

This procedure adjusts the probe compensation output voltage of the DSO module.

SW test names	PROBE_COMP_CAL
Equipment required	Digital multimeter (item 24) Precision BNC cable (item 31) Dual banana-to-BNC adapter (item 25)
Prerequisites	Warm-up time: 30 minutes The logic analyzer application is not running Test equipment connected as shown in Figure 8–14 Power-up diagnostics pass INTERNAL_CAL test pass

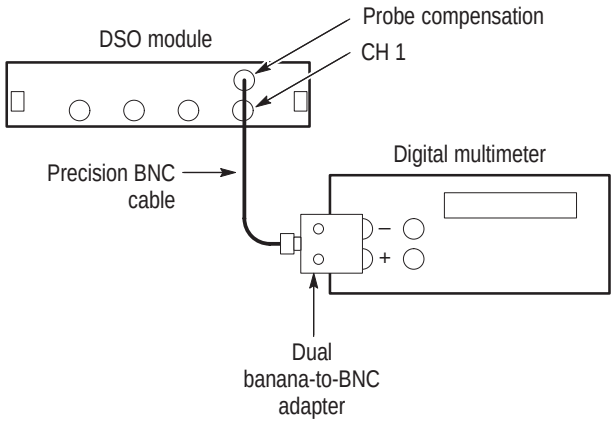

Figure 8–14: Initial setup for the probe compensation test

1. Verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run the test for the DSO module.
3. Verify no failures occur for each test. If a test continues to fail, check the *Troubleshooting* section on page 8–29.

Completing the Adjustment Steps

After completing the adjustments, obtain a copy of the test results and verify that all tests passed. Refer to *Retrieving Test Data from the PV/Adjust Software* on page 1–15 for instructions on obtaining test data.

Run the *Performance Verification Procedures* to verify that all the parameters are within the allowable specifications as listed in the *TLA 700 Series Logic Analyzer User Manual*.

Pattern Generator Module

Pattern Generator Module Functional Verification

This section contains instructions for performing the functional verification procedures for the TLA7PG2 Pattern Generator modules, the P6470 TTL/CMOS Pattern Generator Probes, and the P6471 ECL Pattern Generator Probes. These procedures provide an easy way to check the basic functionality of the modules and probes.

Table 9–1 lists the functional verification procedures available for the pattern generator modules and probes. Note that probes must be attached for all tests except for the extended diagnostics. The columns under the headings *Required for P6470* or *Required for P6470* indicate that the tests do not necessarily verify the functionality of the probes. However the probes are needed to send the signals to the Termination board.

Table 9–1: Pattern generator module functional verification procedures

Test	Setup file name	Required for P6470	Required for P6471	Termination board required
Extended diagnostics	N.A.	No	No	No
Internal clock frequency	TP1CLK.TPG	Yes	Yes	Yes
External clock input (Half, Normal)	TP2EXCLK.TPG	Yes	Yes	Yes
External clock input (Half, Invert)	TP3EXCLK.TPG	No	No	Yes
External clock input (Full)	TP4EXCLK.TPG	No	No	Yes
Sequence and data output (probe A)	TP5PG.TPG	Yes	Yes	Yes
Sequence and data output (probe B)	TP6PG.TPG	No	No	Yes
Sequence and data output (probe C)	TP7PG.TPG	No	No	Yes
Sequence and data output (probe D)	TP8PG.TPG	No	No	Yes
Merge operation	TP9PG.TPG	No	No	Yes
Deskew function	TP10DSKW.TPG	No	No	Yes
Inhibit function (by event using Signal1 Output and Signal1 Input)	TP12INH.TPG	Partially	No	Yes
Inhibit function(by external inhibit input)	TP13INH.TPG	Partially	No	Yes
Inhibit function (by data)	TP14INH.TPG	Partially	No	Yes

If any checks within this section fail, refer to the *Troubleshooting* chapter in the *TLA7PG2 Pattern Generator Module Service Manual* for assistance. Failed tests indicate the instrument needs to be serviced.

Test Equipment

You will need the following equipment to complete the functional verification procedure:

- TLA 700 Series Logic Analyzer mainframe with one pattern generator module installed (more modules are required to check the merged functionality)
- Two termination boards (with an external power supply)
- Other test equipment as listed at the beginning of each check.

Setup

Refer to Figure 9–1 and the following steps to connect the test equipment to the termination board.

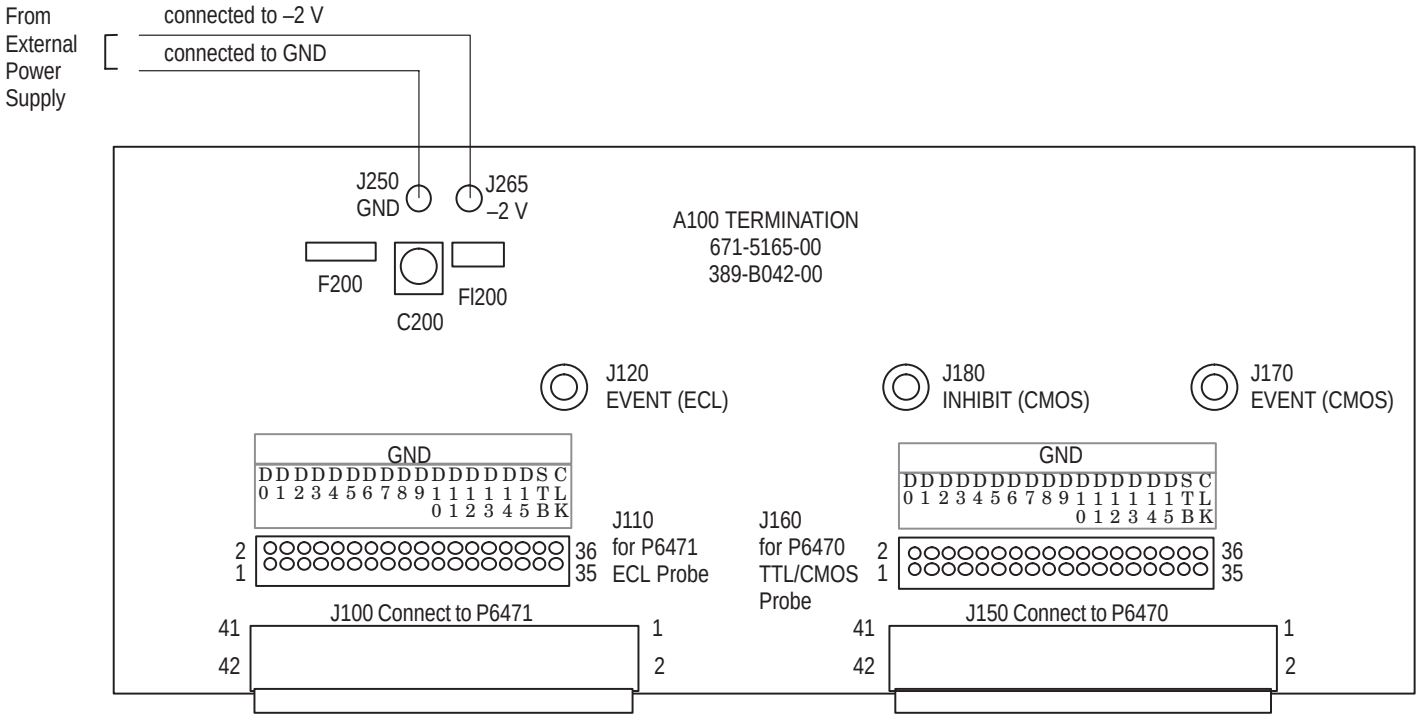

Figure 9–1: Termination Board

Connect the Power Supply (P6471 ECL Probe Only)

Follow the steps below to connect the termination board to an external power supply (the –2 V supply is required to test the P6471 ECL probe):

1. Connect the –2 V output of the power supply to J265 on the termination board.
2. Connect the power supply ground to J250 on the termination board.

Connect the Probes to the Termination Board

Position the termination board and the probes so that the probe labels are on top. The follow steps depend on which probe you are using.

- Connect the P6470 TTL/CMOS probe to J150 on the termination board.
- Connect the P6471 ECL probe to J100 on the termination board.

You can connect or disconnect the probes to or from the termination board while the power is on.

Connect the Probe Event and Inhibit Inputs

The following connections are used to input signals from the function generator:

- **External Event Input.** Use J120 on the termination board for the P6471 ECL probe.
- **External Event Input.** Use J170 on the termination board for the P6470 TTL/CMOS probe.
- **External Inhibit Input.** Use J180 on the termination board for the P6470 TTL/CMOS probe.

Connect the Oscilloscope to the Termination Board

The following connections are used to connect the termination board to the oscilloscope:

- Use J110 on the termination board for the P6471 ECL probe.
- Use J160 on the termination board for the P6470 TTL/CMOS probe.
- Use J110 upper pins (2 through 36) for GND.
- Use TP100, TP110, TP150, and TP160 on the termination board for oscilloscope probing.

Install the Pattern Generator Module

If you have not already installed the pattern generator module in the TLA700 mainframe, complete the following steps:

CAUTION. *Power off the TLA700 mainframe before removing or installing the pattern generator module. Power off the mainframe while connecting or disconnecting the probes to the pattern generator module. You can damage the pattern generator if you connect or disconnect the probe while the mainframe is powered on.*

1. Power off the TLA700 mainframe.
2. Install the pattern generator module in the TLA700 mainframe.
   a. If you are testing a single module, install the module in any slot.
   b. If you are testing multiple modules, install one pattern generator module in the lower-numbered slot. Install the pattern generator module to be tested in the adjacent higher-numbered slot.
3. Connect the P6470 or P6471 probes to the Probe-A connector of the pattern generator module using the through the probe cable. Connect four sets of the same probe to the pattern generator module.
4. Power on the mainframe and test equipment and allow a 30-minute warm up before continuing with any procedures in this section.

Module Self Tests and Power-On Diagnostics

During power-on, the installed modules perform an internal self test to verify basic functionality. No external test equipment is required. The self tests require only a few seconds per module to complete. The front-panel indicators may blink during the self test. Table 9–2 summarizes the function of each indicator.

Table 9–2: Front panel indicators

Function	Description
Ready LED (green)	The Ready LED illuminates when the module is ready for operation.
Accessed LED (amber)	The Accessed LED illuminates each time the mainframe communicates with the pattern generator module.
Output LED (amber)	The Output LED illuminates while the probe is asserting a high or low level at the output pins. It will not illuminate while the output pins are in the high impedance state when the HI-Z on Stop function is active. If you have a P6471 ECL probe, the LED will always be illuminated because the probe does not support Hi-Z on Stop.

Table 9–2: Front panel indicators (Cont.)

Function	Description
Started LED (green)	The Started LED illuminates while the pattern generator runs or is waiting for an event.
Waiting LED (green)	The Waiting LED illuminates while the pattern generator is waiting for an event.

Next, the power-on diagnostics are run. If any self tests or power-on diagnostics fail, the instrument displays the Diagnostics property sheet. If any diagnostics fail, run the extended diagnostics to help isolate the problem.

Extended Diagnostics

The following procedure checks the basic functionality of pattern generator module using the extended diagnostics. Before beginning this procedure, be sure that no active signals are applied to the instrument. Certain diagnostic tests may fail if signals are applied to the probe during the test.

1. In the pattern generator application, go to the System menu and select System Diagnostics.
2. Click the Extended Diagnostics tab.
3. Select the top level test of the pattern generator module and then click the Run button.

   The diagnostics will perform each one of the tests listed in the menu under the module selection. All tests that displayed an Unknown status will change to a Pass or Fail status depending on the outcome of the tests.
4. Scroll through the test results and verify all tests pass. If any tests fail, refer to Table 9–3 to identify the fault.

Table 9–3: Extended Diagnostic test Items and faulty component

Test item	Faulty component
ROM Test	A20 CLOCK and VXI I/F board
RAM Test	A20 CLOCK and VXI I/F board
Register Read Test	A20 CLOCK and VXI I/F board or A50 PG board or A90 ECL board or A95 TTL/CMOS board
PLL Lock Test	A20 CLOCK and VXI I/F board

Table 9–3: Extended Diagnostic test Items and faulty component (Cont.)

Test item	Faulty component
Pattern Memory Test	A50 PG board
Sequence Memory Test	A50 PG board
Event Memory Test	A50 PG board
Signal Test	A50 PG board

Using the Software Setup Files

Each of the following procedures uses setups stored on the hard disk drive. For each test, select the appropriate setup file and load it when indicated. To load the setup files, do the following steps:

1. Ensure that the pattern generator application is running.
2. From the pattern application file menu, select Load Module . . . to display the Load Module dialog box.
3. Click the Browse button to display the Open dialog box.
4. Navigate to the folder containing the setup files (C:\Program Files\Tektronix Pattern Generator\PV).
5. Double-click on the test file name. The Open dialog box closes and the Load Module dialog box displays with PG 1 selected in the Modules list.
6. Click OK to load the setup and then click Yes in the Pop-up dialog box when you are asked to load the new system without saving the current setups.
7. Follow the steps under each procedure to complete the check.

Troubleshooting

If any tests fail, use the following steps to troubleshoot problems:

1. Check all test equipment for improper or loose connections.
2. Check that all test equipment is powered on and has the proper warm-up time.
3. Rerun mainframe or module diagnostics.
4. Run the tests a second time to verify the failure.
5. If tests continue to fail, refer to the *TLA7PG2 Pattern Generator Module Service Manual* for corrective action.

Functional Verification Tests

Complete each of the following procedures in sequence. Use the external test equipment together with the tables and illustrations in this section to verify the functionality of the pattern generator modules and probes as indicated.

Internal Clock Frequency

The Internal Clock Frequency test confirms the frequency of the pattern generator module internal clock with the P6470 TTL/CMOS probe or P6471 ECL probe.

Setup files	TP1CLK.TPG
Equipment required	Termination board (item 14) TDS784D Digitizing Oscilloscope (item 6) P6245 1 MΩ 10X Oscilloscope probe (Item 7) Metronix 524B Power supply (item 17)
Prerequisites	Warm-up time: 30 minutes P6470 or P6471 probes connected Test equipment connected as shown in Figure 9–2 Diagnostics pass

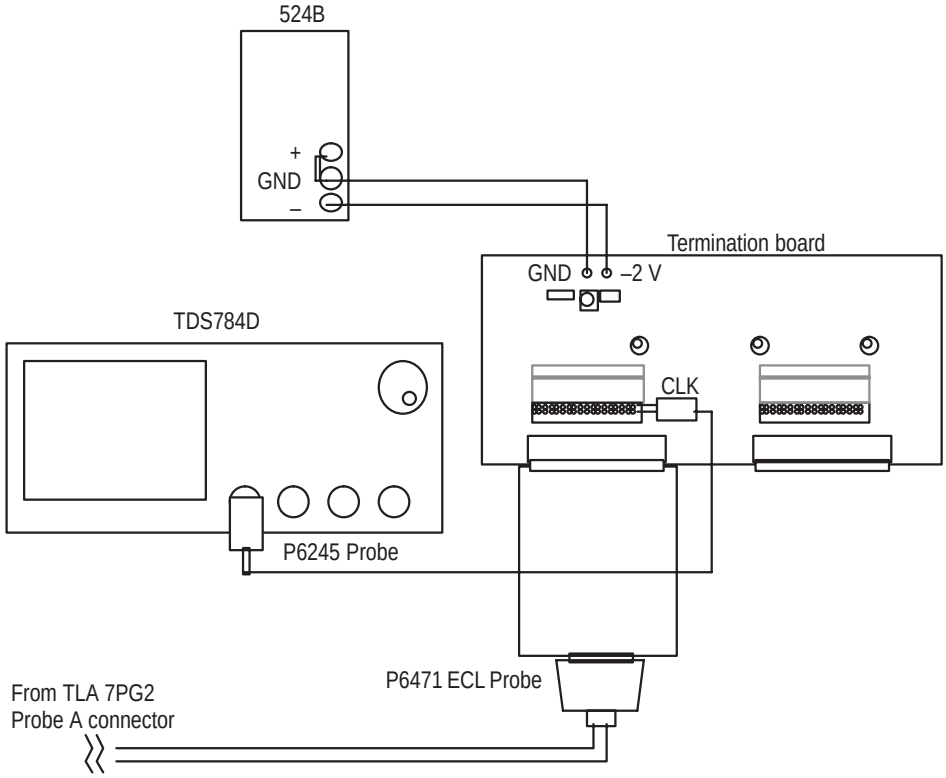

Figure 9–2: Internal Clock Frequency connections

1. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
2. Set the oscilloscope controls as follows:

■ Displayed channel	CH1
■ Vertical axis (CH1)	2 V/div (P6470) 500 mV/div (P6471)
■ Vertical position (CH1)	–2.00 div (P6470) 1.00 div (P6471)
■ Bandwidth	Full
■ Input coupling	DC
■ Input impedance	50 Ω
■ Horizontal axis	1 ns/div
■ Record length	5000

- Trigger mode — NORM
- Trigger Source — CH1
- Trigger Slope — Rise
- Trigger level — 2 V (P6470)
–1.3 V (P6471)
- Trigger coupling — DC
- Trigger position — 50%

3. Load the TP1CLK.TPG module setup file. When the file is loaded, the pattern generator clock period will be set to 3.7313 ns internally.
4. Start the pattern generator.
5. If you are testing the P6471 ECL probe, use the frequency measurement function of the oscilloscope to verify that the frequency of the pattern generator output signal is about 268 MHz.
6. Click the Setup icon in the pattern generator application window and change the internal clock period to 9.99 ns.
7. Verify that the frequency of the pattern generator output signal is 100.1 MHz.
8. Set the pattern generator clock period to 5.0000 μs.
9. Set the oscilloscope Horizontal axis setting to 1.00 μs/div.
10. Verify that the frequency of the pattern generator output signal is 200 kHz.
11. Set the pattern generator clock period to 1.0000 s.
12. Set the oscilloscope Horizontal axis setting to 200 ms/div.
13. Verify that the frequency of the pattern generator output signal is about 1 Hz.
14. Stop the pattern generator.

External Clock Input

The External Clock Input test confirms the external clock input operation of the pattern generator module.

Setup files	TP2EXCLK.TPG, TPEXCLK.TPG, TP3EXCLK.TPG
Equipment required	Termination board (item 14) TDS784D Digitizing Oscilloscope (item 6) P6245 1 MΩ 10X Oscilloscope probe (Item 7) Metronix 524B Power supply (item 17) AFG2020 Function generator (item 16) Two BNC cables (item 18) T-connector (item 19)
Prerequisites	Warm-up time: 30 minutes P6470 or P6471 probes connected Test equipment connected as shown in Figure 9–3 Diagnostics pass

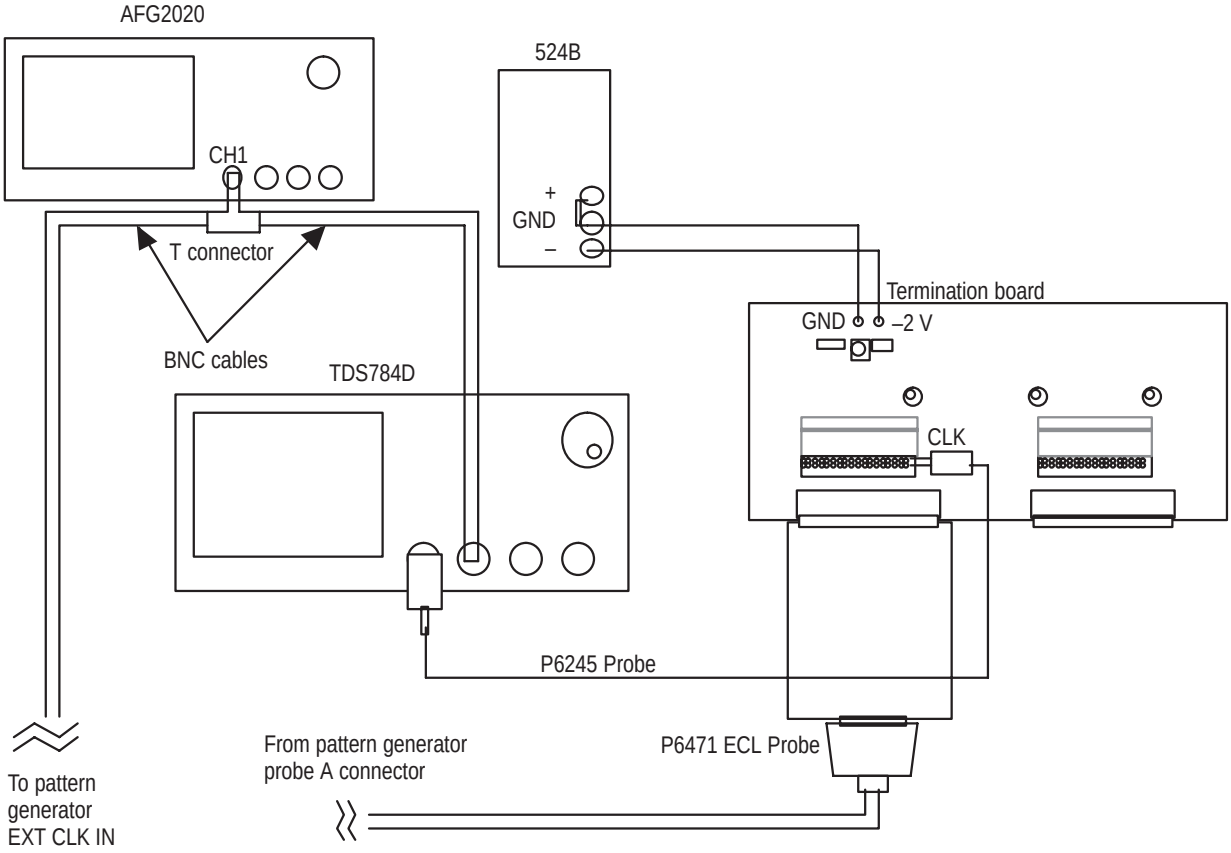

Figure 9–3: External Clock Input connections

1. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
2. Set the oscilloscope controls as follows:

■ Displayed channel	CH1, CH2
■ Vertical axis (CH1)	2 V/div (P6470) 500 mV/div (P6471)
■ Vertical axis (CH2)	500 mV/div
■ Vertical position (CH1)	–2.00 div (P6470) 1.00 div (P6471)
■ Vertical position (CH2)	1.00 div
■ Bandwidth	Full
■ Input coupling (CH1, CH2)	DC

- Input impedance (CH1, CH2) 50 Ω
- Horizontal axis 200 ns/div
- Record length 5000
- Trigger mode NORM
- Trigger Source CH2
- Trigger Slope Rise
- Trigger level 500 mV
- Trigger coupling DC
- Trigger position 50%

3. Set up Channel 1 of the function generator as follows:
   - Waveform Square wave
   - Frequency 1 MHz
   - Amplitude 1 V_{p-p} (50 Ω termination)
   - Offset 500 mV (50 Ω termination)
   - CH1 ON
4. Load the TP2EXCLK.TPG module setup file.
5. Start the pattern generator.
6. Verify that the leading edge of the 1 MHz clock signal is synchronized with the leading edge of the Ch2 waveform.
7. Stop the pattern generator.
8. Load the TP3EXCLK.TPG module setup file.
9. Start the pattern generator.
10. Verify that the trailing edge of the 1 MHz clock signal is synchronized with the trailing edge of the Ch2 waveform.
11. Stop the pattern generator.
12. Load the TP4EXCLK.TPG module setup file.
13. Start the pattern generator.

14. Verify that the leading edge of the 1 MHz clock signal is synchronized with the leading edge of the Ch2 waveform.

15. Stop the pattern generator.

Sequence and Data Output

The Sequence and Data Output test confirms that the pattern generator sends the proper sequences and data to the probes. This check also verifies the probe operation.

Setup files	TP5PG.TPG, TP6PG.TPG, TP7PG.TPG, TP8PG.TPG
Equipment required	Termination board (item 14) TDS784D Digitizing Oscilloscope (item 6) Three P6245 1 MΩ 10X Oscilloscope probes (Item 7) Metronix 524B Power supply (item 17) AFG2020 Function generator (item 16) One BNC cable (item 18)
Prerequisites	Warm-up time: 30 minutes P6470 or P6471 probes connected Test equipment connected as shown in Figure 9–4 Diagnostics pass

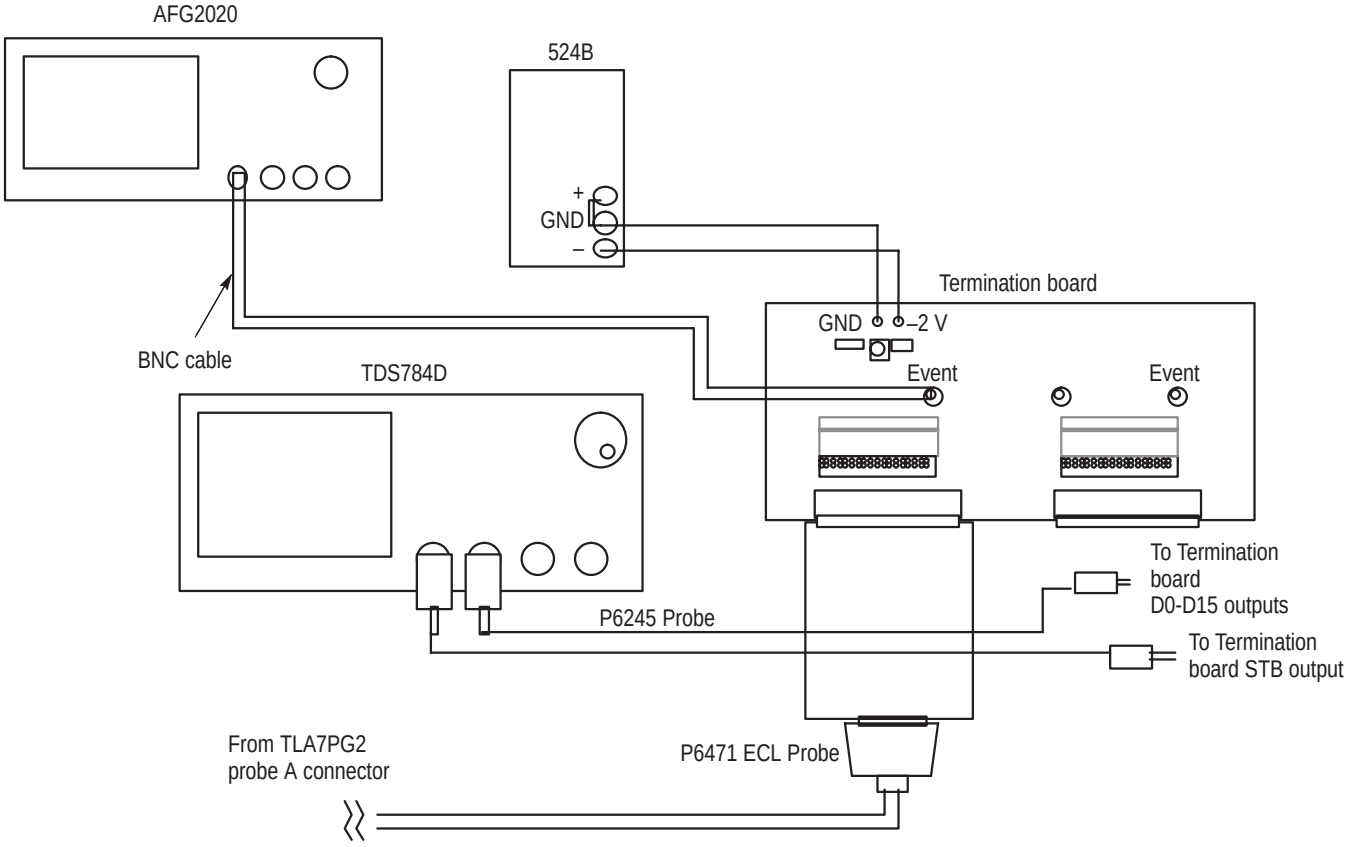

Figure 9–4: Sequence and Data Output connections

1. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
2. Set the oscilloscope controls as follows:

■ Displayed channel	CH1, CH2
■ Vertical axis (CH1, CH2)	5 V/div (P6470) 500 mV/div (P6471)
■ Vertical position (CH1)	2.00 div (P6470) 5.00 div (P6471)
■ Vertical position (CH2)	0.00 div (P6470) 3.00 div (P6471)
■ Bandwidth	Full
■ Input coupling (CH1, CH2)	DC
■ Input impedance (CH1, CH2)	50 Ω

- Horizontal axis — 1 µs/div
- Record length — 5000
- Trigger mode — AUTO
- Trigger Source — CH1
- Trigger Slope — Rise
- Trigger level — 2 V (P6470), –1.3 V (P6471)
- Trigger coupling — DC
- Trigger position — 50%

3. Set up Channel 1 of the function generator as follows:
   - Waveform — Square wave
   - Frequency — 200 kHz
   - Amplitude — 2 V_{p-p} (50 Ω termination, P6470); 500 mV_{p-p} (50 Ω termination, P6471)
   - Offset — 1 V (50 Ω termination, P6470); –650 mV (50 Ω termination, P6471)
   - CH1 — ON
4. Load the TP5PG.TPG module setup file.
5. Verify that the front panel Accessed indicator blinks on the pattern generator module.
6. Start the pattern generator.
7. Verify that the CH1 waveforms are similar to the waveforms shown in Figure 9–5.
8. Connect the CH2 Probe on the oscilloscope to the D0 connector on the termination Board. Verify that the output signal data pattern is similar to the waveform shown in Figure 9–5. Repeat this procedure on the output signals from the D1 through the D15 connector.
9. Stop the pattern generator.

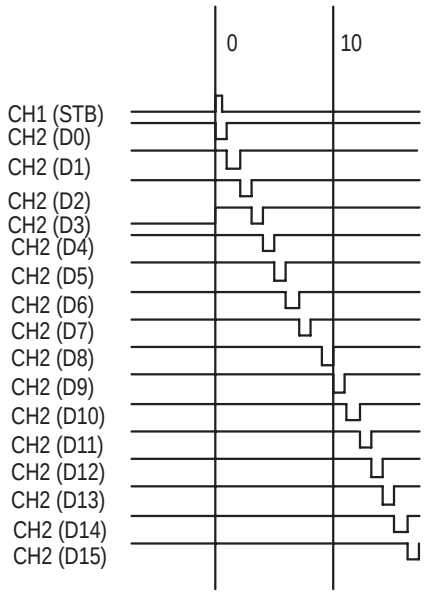

Figure 9–5: Timing Chart

10. Connect Probe B to the termination board.

11. Load the TP6PG.TPG module setup file.

12. Repeat steps 6 through 9.

13. Connect Probe C to the termination board.

14. Load the TP7PG.TPG module setup file.

15. Repeat steps 6 through 9.

16. Connect Probe D to the termination board.

17. Load the TP8PG.TPG module setup file.

18. Start the pattern generator.

19. Verify that the CH1 waveforms are similar to the waveforms shown in Figure 9–6.

20. Connect the CH2 Probe of the oscilloscope to the D0 connector on the termination Board. Verify that the output signal data pattern is similar to the waveform shown in Figure 9–6. Repeat this procedure on the output signals from the D1 through the D15 connector.

21. Verify that the Ready, Output**,** and Started front panel indicators are illuminated and the Waiting front panel indicator blinks while the system is operating.

22. Stop the pattern generator.

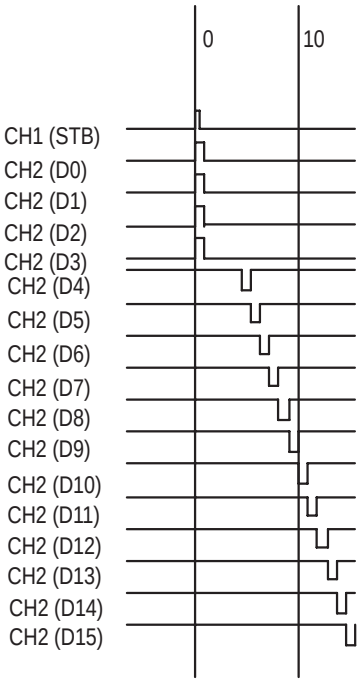

Figure 9–6: Timing Chart

Merge Operation

This check confirms that the pattern generator merges properly.

Setup files	TP9PG.TPG
Equipment required	Two termination boards (item 14) TDS784D Digitizing Oscilloscope (item 6) Three P6245 1 MΩ 10X Oscilloscope probes (Item 7) Metronix 524B Power supply (item 17) AFG2020 Function generator (item 16) One BNC cable (item 18)
Prerequisites	Warm-up time: 30 minutes Pattern generator modules merged, module under test in the higher-numbered slot P6470 or P6471 probes connected Test equipment connected as shown in Figure 9–7 Diagnostics pass

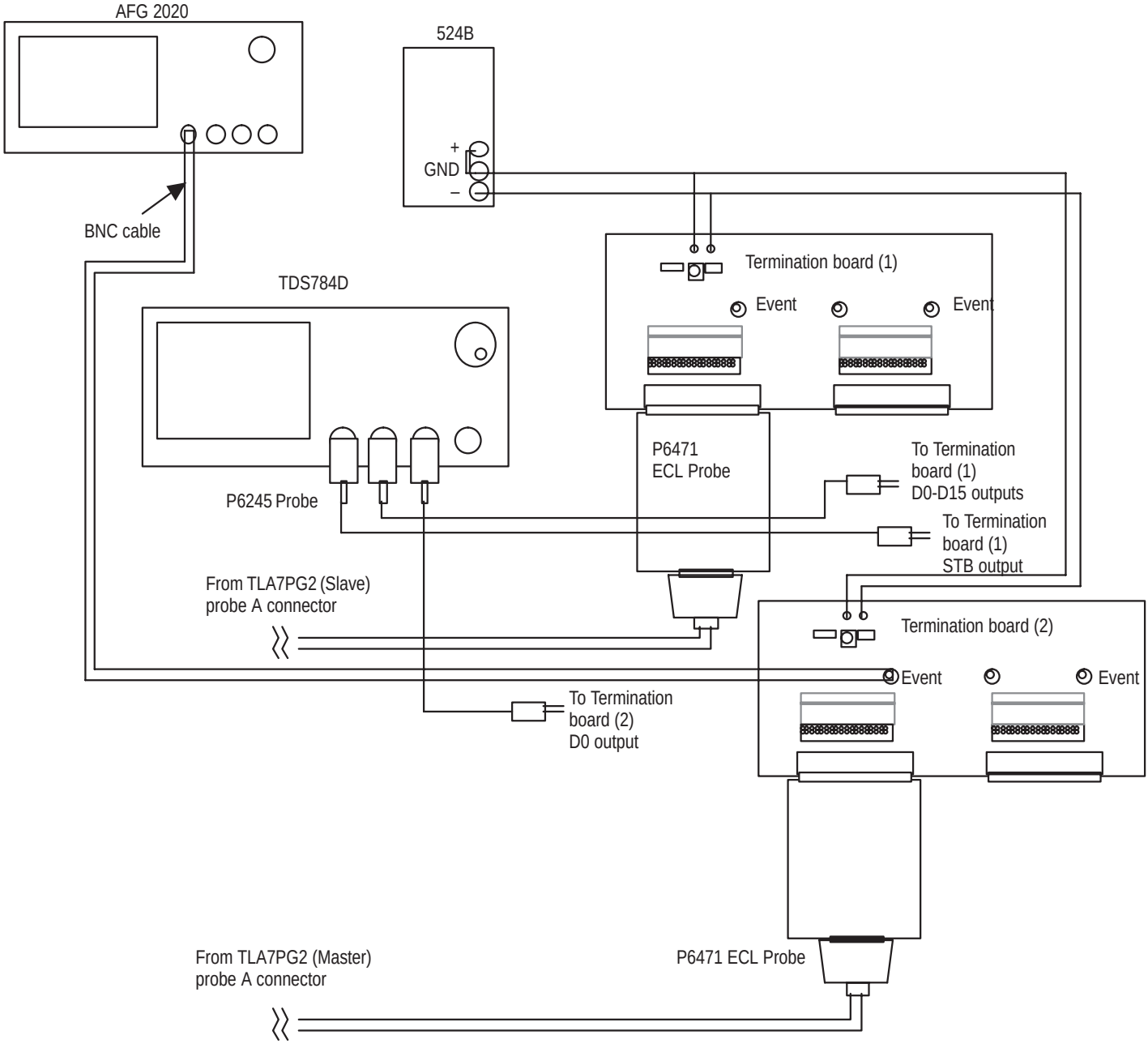

Figure 9–7: Merge operation Connections

1. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
2. Set the oscilloscope controls as follows:

■ Displayed channel	CH1, CH2, CH3
■ Vertical axis (CH1, CH2, CH3)	5 V/div (P6470) 1 V/div (P6471)
■ Vertical position (CH1)	2.50 div (P6470) 4.00 div (P6471)
■ Vertical position (CH2)	0.50 div (P6470) 2.00 div (P6471)
■ Vertical position (CH3)	–1.50 div (P6470) 0.00 div (P6471)
■ Bandwidth	Full
■ Input coupling	DC
■ Input impedance	50 Ω
■ Horizontal axis	1 μs/div
■ Record length	5000
■ Trigger mode	AUTO
■ Trigger Source	CH1
■ Trigger Slope	Rise
■ Trigger level	2 V (P6470), –1.3 V (P6471)
■ Trigger coupling	DC
■ Trigger position	50%

3. Set up Channel 1 of the function generator as follows:

■ Waveform	Square wave
■ Frequency	200 kHz
■ Amplitude	2 V_{p-p} (50 Ω termination) (P6470) 500 mV_{p-p} (50 Ω termination) (P6471)
■ Offset	1 V (P6470) –650 mV (P6471)

- CH1 ON

4. If you have not already done so, complete the following steps to merge the pattern generator module under test to the reference module:

   a. Select System Configuration from the System menu in the pattern generator application.

   b. Click the Merge button between the reference module and the module under test to merge the two modules. (Figure 9–8 shows an example where PG6 consists of two merged modules, while PG3, PG4, and PG5 are unmerged modules as; note the merge buttons.)

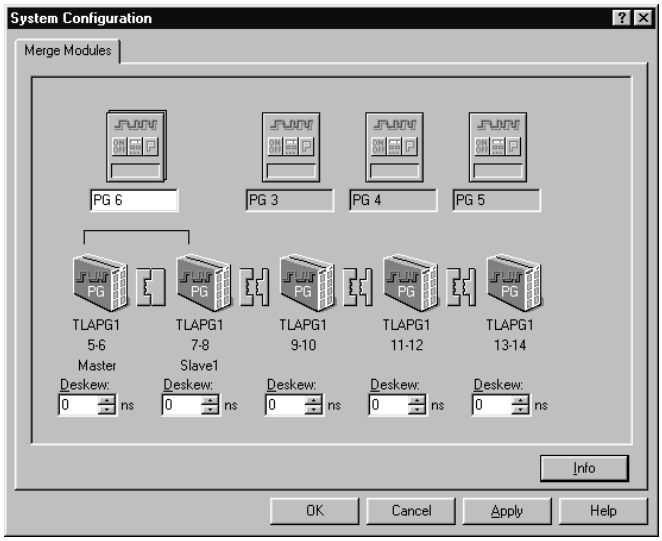

Figure 9–8: Merged and unmerged modules in the Merge Modules window

   c. Click OK to save the changes.

5. Load the TP9PG.TPG module setup file.

6. Start the pattern generator.

7. Verify that the CH1 waveforms are similar to the waveforms shown in Figure 9–9. Notice the position of the strobe pulse in the figure.

8. Connect the CH2 oscilloscope probe to the D0 connector on the termination Board. Verify that the output signal data pattern is similar to the waveform shown in Figure 9–9. Repeat this procedure for output signals from D1 through D15.

9. Stop the pattern generator.

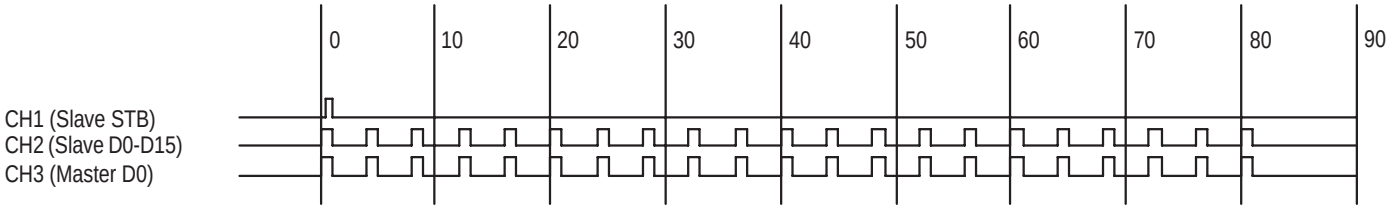

Figure 9–9: Timing Chart

Deskew Function

This check confirms the deskew function of the pattern generator module.

Setup files	TP10DSKW.TPG
Equipment required	Two termination boards (item 14) TDS784D Digitizing Oscilloscope (item 6) P6245 1 MΩ 10X Oscilloscope probe (Item 7) Metronix 524B Power supply (item 17)
Prerequisites	Warm-up time: 30 minutes Pattern generator modules merged, module under test in the higher-numbered slot P6470 or P6471 probes connected Test equipment connected as shown in Figure 9–10 Diagnostics pass

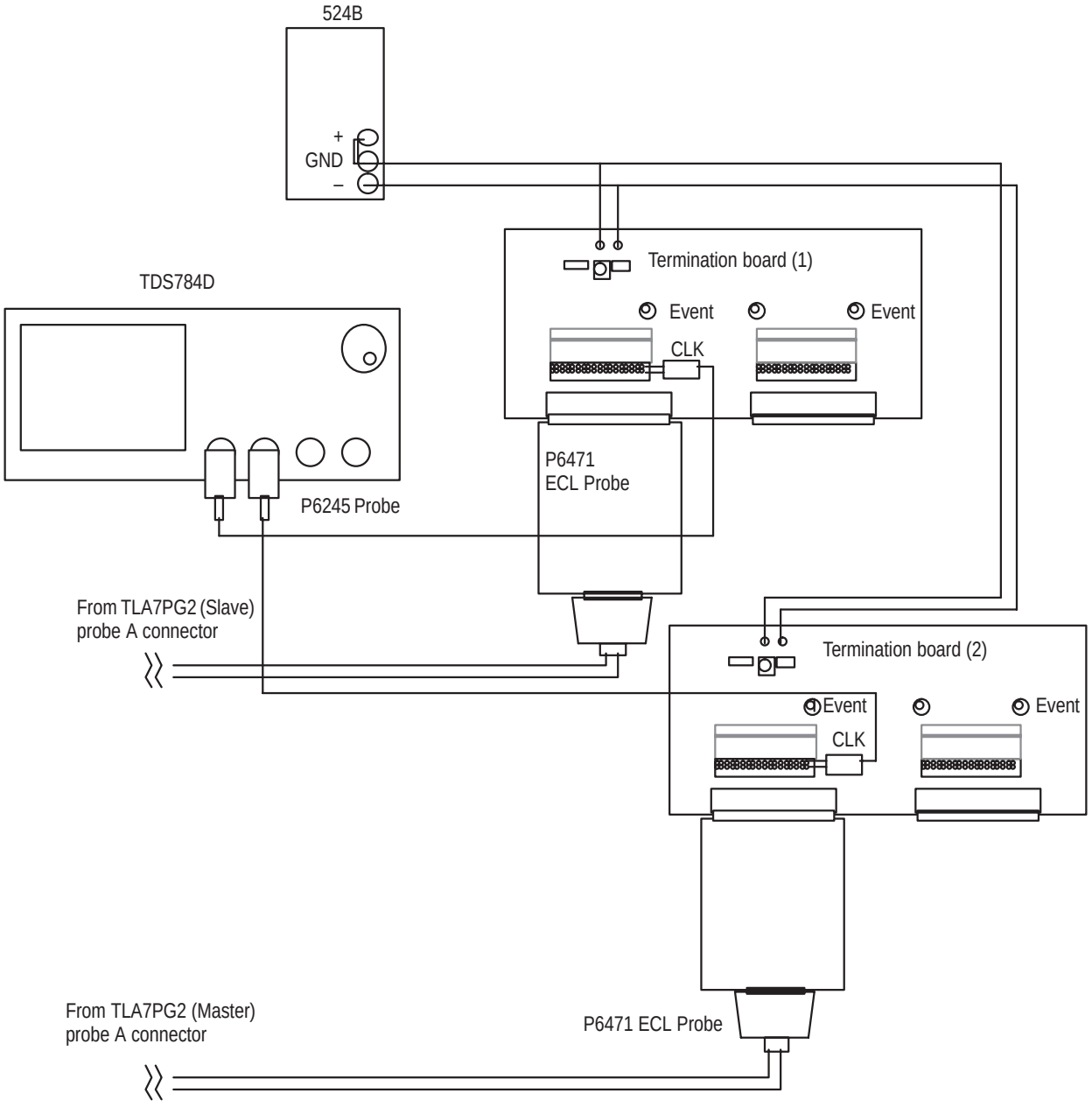

Figure 9–10: Deskew function connections

1. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
2. Set the oscilloscope controls as follows:

■ Displayed channel	CH1, CH2
■ Vertical axis (CH1, CH2)	2 V/div (P6470) 500 mV/div (P6471)
■ Vertical position (CH1)	–1.00 div (P6470) 4.00 div (P6471)
■ Vertical position (CH2)	–1.00 div (P6470) 2.00 div (P6471)
■ Bandwidth	Full
■ Input coupling	DC
■ Input impedance	50 Ω
■ Horizontal axis	1 ns/div
■ Record length	5000
■ Trigger mode	NORM
■ Trigger Source	CH2
■ Trigger Slope	Rise
■ Trigger level	2 V (P6470), –1.3 V (P6471)
■ Trigger coupling	DC
■ Trigger position	50%

3. Load the TP10DSKW.TPG module setup file.
4. Select System Configuration in the pattern generator application to display the Merge Modules window.
5. Set the Deskew setting for Slave1 module to 1.5 ns.
6. Click OK to save the changes and to close the window.
7. Start the pattern generator.
8. Record the delay time from the leading edge of the CH1 waveform to the leading edge of the CH2 waveform (T1).
9. Stop the pattern generator.

10. Select System Configuration in the pattern generator application to display the Merge Modules window.
11. Set the deskew value of the Slave1 module to –1.5 ns.
12. Click OK to save the changes and to close the window.
13. Start the pattern generator.
14. Write down the delay time from the leading edge of the CH1 waveform to the leading edge of the CH2 waveform (T2).
15. Stop the pattern generator.
16. Verify that T1 minus T2 is approximately 2 ns.

Inhibit Function

This check confirms the Inhibit function of the pattern generator module and the P6470 TTL/CMOS pattern generator probes.

Setup files	TP12INH.TPG, TP13INH.TPG, TP14INH.TPG
Equipment required	Termination board (item 14) TDS784D Digitizing Oscilloscope (item 6) P6245 1 MΩ 10X Oscilloscope probe (Item 7) AFG2020 Function generator (item 16) Metronix 524B Power supply (item 17) One BNC cable (item 18)
Prerequisites	Warm-up time: 30 minutes Pattern generator modules *not* merged P6470 or P6471 probes connected Test equipment connected as shown in Figure 9–11 Diagnostics pass

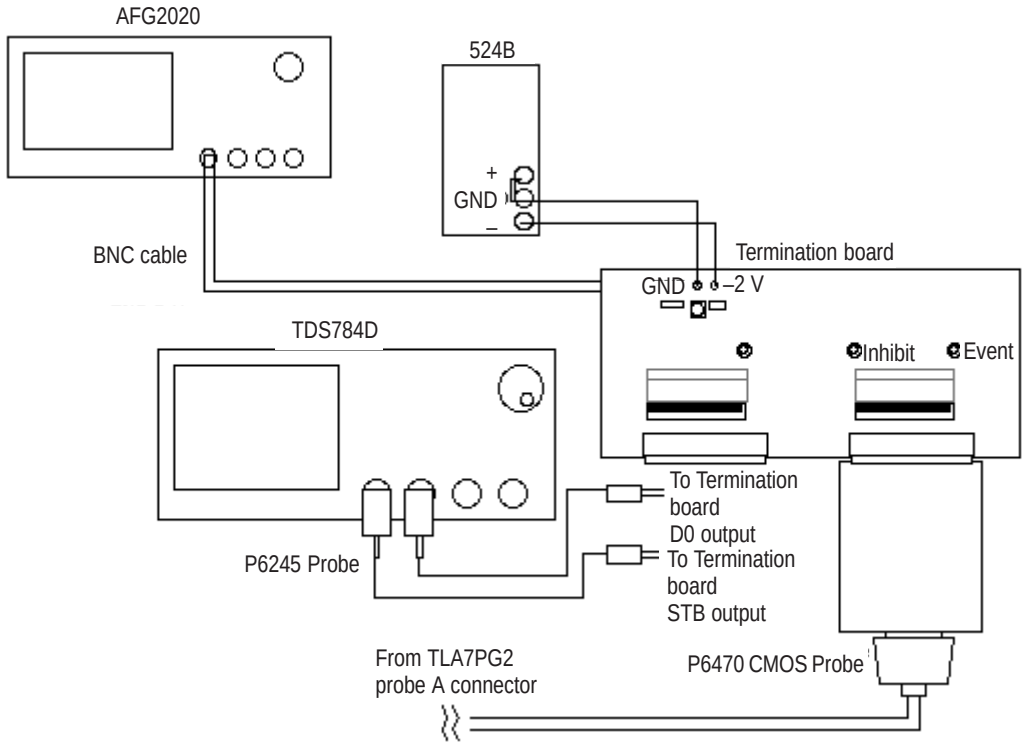

Figure 9–11: Inhibit function connections

1. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
2. Set the oscilloscope controls as follows:
   - Displayed channel — CH1, CH2
   - Vertical axis (CH1, CH2) — 2 V/div
   - Vertical position (CH1) — 1.00 div
   - Vertical position (CH2) — –3.00 div
   - Bandwidth — Full
   - Input coupling — DC
   - Input impedance — 50 Ω
   - Horizontal axis — 1 ms/div
   - Record length — 5000
   - Trigger mode — NORM

- Trigger Source CH2
- Trigger Slope Rise
- Trigger level 2 V
- Trigger coupling DC
- Trigger position 50%

3. Set up Channel 1 of the function generator as follows:

- Waveform Square wave
- Frequency 500 Hz
- Amplitude 2 V_{p-p} (50 Ω termination)
- Offset 1 V (50 Ω termination)
- CH1 ON

4. If you have not already done so, complete the following steps to unmerge the pattern generator modules:

a. Select System Configuration from the System menu in the pattern generator application.

b. Click the Merge button between the merged modules to unmerge the two modules.

c. Click the OK button.

5. Load the TP12INH.TPG module setup file.

6. Start the pattern generator.

7. Verify that the CH2 output signal has a 500 Hz clock pattern.

8. Verify that 1 ms of low level and 1 ms of burst data are output alternately on CH1.

9. Repeat step 7 for Probe B, Probe C, and Probe D.

10. Stop the pattern generator.

11. Connect a BNC Cable to J180 (Inhibit) on the termination board.

12. Connect Probe A to the termination Board.

13. Load the TP13INH.TPG module setup file.

14. Start the pattern generator.

15. Verify that a 500 Hz clock pattern appears on CH2 and that the high and low levels are approximately 5 V and 0 V.
16. Verify that 1 ms of low level and 1 ms of burst data are output alternately on CH1.
17. Repeat step 7 for Probe B, Probe C, and Probe D.
18. Stop the pattern generator.
19. Disconnect Probe D from the termination board.
20. Connect Probe A to the termination Board.
21. Disconnect the BNC Cable from the termination Board.
22. Load the TP14INH.TPG module setup file.
23. Start the pattern generator.
24. Verify that the output signal on Ch2 has a 500 Hz clock pattern.
25. Verify that 1 ms of low level and 1 ms of burst data are output alternately on CH1.
26. Repeat step 7 for Probe B, Probe C, and Probe D.
27. Stop the pattern generator.

This completes the functional verification of the pattern generator module and the pattern generator probes.

Pattern Generator Module Certification

There are no certifiable parameters for the TLA7P2 Pattern Generator modules or for the P6470 and P6471 Pattern Generator probes.

Pattern Generator Module Performance Verification

This section contains procedures to verify that the TLA7PG2 Pattern Generator module perform as warranted. Verify the instrument performance whenever the accuracy or function of the module or probes are in question or as part of an annual calibration/certification.

As a general rule, these tests should be done once a year.

Prerequisites

The tests in this section comprise an extensive, valid confirmation of performance and functionality when the following requirements are met:

- The pattern generator module and probes pass all of the functional tests in the *Pattern Generator Module Functional Verification* section.
- The PV/Adjust software must be loaded on the hard disk drive. Refer to *Software Installation and Removal Instructions* on page 1–8.
- The pattern generator module must be installed in a mainframe, operating for at least 30 minutes, and operating at an ambient temperature between +20° C and +30° C. (Refer to *Setups* on page 9–2 in the *Pattern Generator Module Functional Verification* section for information on equipment setups.)
- The instrument must be in an operating environment within the limits described in the *Specifications* section of the *TLA 700 Series Logic Analyzer User Manual*.

Tests Performed

This sections verifies the maximum operating frequency of the pattern generator module.

Test Equipment

These procedures use external, traceable signal sources to directly test the characteristics that are designated as checked (✓) in the *Specifications* section of the *Tektronix Logic Analyzer Family User Manual*. In addition to the basic setup, you will need some of the equipment shown in Table 1–3 on page 1–5 to complete the performance verification procedures. Use Table 1–3 for equipment specifications. If you substitute equipment, always choose instruments that meet or exceed the minimum requirements specified.

Performance Verification Tests

Use the following tables and figures to set up and execute each procedure.

Maximum Operating Frequency

This procedure verifies the maximum operating frequency of the pattern generator module. The procedure uses four separate test files, one for each probe connector as indicated below.

SW test names	TP15PVP.TPG (Performance check using probe A) TP16PVP.TPG (Performance check using probe B) TP17PVP.TPG (Performance check using probe C) TP18PVP.TPG (Performance check using probe D)
Equipment required	Termination board (item 14) Function Generator (item 16) TDS784D Digitizing Oscilloscope (item 6) P6245 1 MΩ 10X Oscilloscope probe (Item 7) BNC cable (item 18) Metronix 524B Power supply (item 17)
Prerequisites	Warm-up time: 30 minutes P6470 or P6471 probes connected Test equipment connected as shown in Figure 9–12 Functional Verifications pass Diagnostics pass

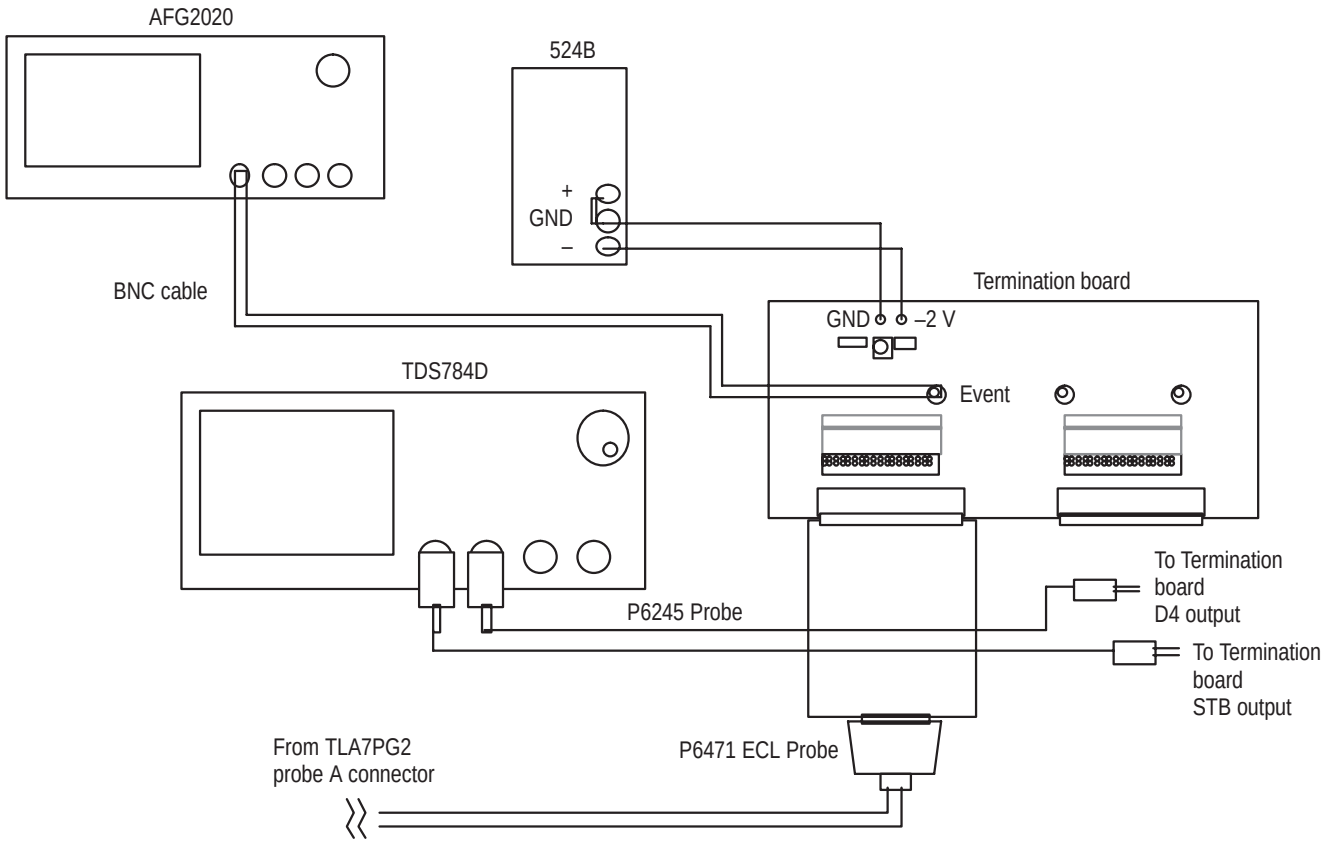

Figure 9–12: Maximum Operating Frequency Connections (Example)

1. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
2. Set the oscilloscope controls as follows:

■ Displayed channel	CH1, CH2
■ Vertical axis (CH1, CH2)	5 V/div (P6470) 1 V/div (P6471)
■ Vertical position (CH1)	2.00 div (P6470) 4.00 div (P6471)
■ Vertical position (CH2)	0 div (P6470) 2.00 div (P6471)
■ Bandwidth	Full
■ Input coupling (CH1, CH2)	DC
■ Input impedance (CH1, CH2)	50 Ω

- Horizontal axis 12.5 ns/div
- Record length 5000
- Trigger mode AUTO
- Trigger Source CH1
- Trigger Slope Rise
- Trigger level 2 V (P6470)
–1.3 V (P6471)
- Trigger coupling DC
- Trigger position 50%

3. Set up Channel 1 of the function generator as follows:

- Waveform Square wave
- Frequency 500 kHz
- Amplitude 2 V p-p (50 Ω termination) (P6470)
500 mV p–p (50 Ω termination) (P6471)
- Offset 1 V (50 Ω termination) (P6470),
–650 mV (50 Ω termination) (P6471)
- CH1 ON

4. Load the TP15PVP.TPG module setup file.

After the file is loaded, the TLA7PG2 clock periods is set to 7.4627 ns.

5. Start the pattern generator.

6. Verify that the data pattern output from the pattern generator probes is similar to the waveform in Figure 9–13 (ignore the small amount of timing skew between the channels).

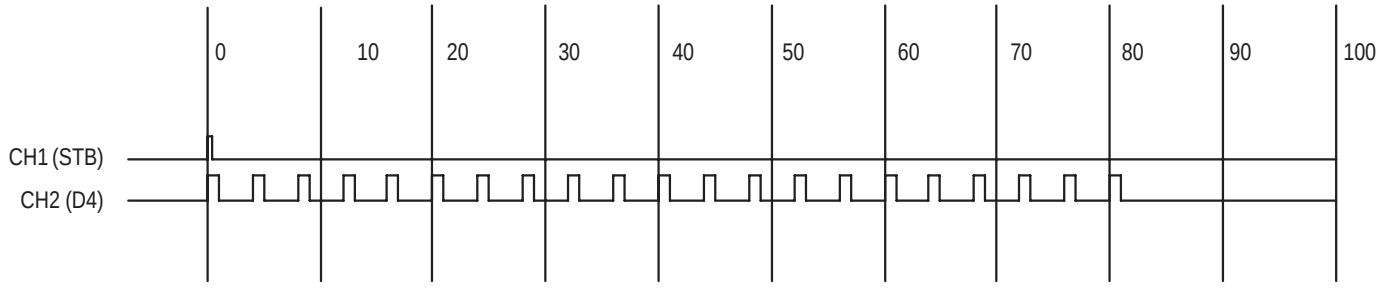

Figure 9–13: Timing chart for the maximum operating frequency check

7. Stop the pattern generator.
8. Connect Probe B to the Termination board.
9. Load the TP16PVP.TPG module setup file.
10. Repeat steps 5 through 7.
11. Connect Probe C to the Termination board.
12. Load the TP17PVP.TPG module setup file.
13. Repeat steps 5 through 7.
14. Connect Probe D to the Termination board.
15. Load the TP18PVP.TPG module setup file.
16. Repeat steps 5 through 7.

Pattern Generator Module Adjustment Procedure

There are no adjustments for the TLA7PG2 Pattern Generator modules or for the P6470 and P6471 Pattern Generator probes.

Appendices

Appendix A: Specifications

The following table lists the specifications for the adjustment/verification fixture. This fixture is used to verify the specifications for the logic analyzer. Specifications marked with the ✓ symbol are checked in the *Performance Verification* Procedures in the adjustment/verification fixture section.

Table A–1: Adjustment/verification fixture specifications

Characteristic	Description
Instrument characteristics	
Number of data outputs	
For P6417 Probes	18 grouped in two groups of eight and one group of two
For P6418 Probes	18 grouped in two groups of eight and one group of two
For P6434 Probes	36 grouped in one connector
Number of setup and hold clock outputs	
For P6417 Probes	Two grouped in one group of two
For P6418 Probes	Two grouped in one group of two
For P6434 Probes	One clock
Number of DC threshold outputs	
For P6417 Probes	16 grouped in two groups of eight and one group of two
For P6418 Probes	16 grouped in two groups of eight and one group of two
For P6434 Probes	36 grouped in one connector
External clock in	External clock input provided by user through a BNC connector
DC threshold input	External input provided by user through a BNC connector
DC power in	Provided by a wall transformer DC power supply (9 V to 12 V DC)
V_{DD} DC level (*typical)*	+5 V referenced to V_{EE}
V_{DD} to analog ground level (*typical)*	+2 V referenced to ground (GND)
V_{DD} switcher noise (*typical)*	50 mV_{p-p} (measured at C17)
✓ Internal clock frequency	50.065 MHz ±0.01%
Output electrical characteristics	
Data/clock output amplitude	10K Motorola ECLinPS family outputs
DC threshold output	Output equals user-applied input

Table A–1: Adjustment/verification fixture specifications (Cont.)

Characteristic	Description
Input requirements	
External Clock input	1.0 V_{p-p} centered around the fixture ground. Specification is valid between 5 MHz and 210 MHz
DC power in	12 Volts DC at 1.5 A. Power is provided by one of the following power supply wall plugs: 119-4855-00, 119-4856-00, 119-4859-00, and 119-4857-00
DC threshold input	Input not greater than ±5 V ground referenced
Output timing	
✓ Data output (channel-to-channel skew)	50 ps (all channels within 50 ps relative to each other)
✓ Setup clock output timing	Adjusted for +3.0 ns (setup) ±100 ps, referenced to one of the data outputs
✓ Hold clock output timing	Adjusted for 0.0 ns (hold) ±100 ps, referenced to one of the data outputs
Minimum data output pulse width	Adjusted for 2.0 ns ±100 ps (jumpered in minimum pulse width mode)
Fuse rating	
Recommended replacement fuse	1.5 AF, 125 V, Tektronix part number 159-5009-00

Appendix B: Replaceable Parts

This section contains a list of the replaceable modules for the adjustment/verification fixture. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Module Servicing

Modules can be serviced by selecting one of the following three options. Contact your local Tektronix service center or representative for repair assistance.

Module Exchange. In some cases you may exchange your module for a remanufactured module. These modules cost significantly less than new modules and meet the same factory specifications. For more information about the module exchange program, call 1-800-TEK-WIDE, extension 6630.

Module Repair and Return. You may ship your module to us for repair, after which we will return it to you.

New Modules. You may purchase replacement modules in the same way as other replacement parts.

Using the Replaceable Parts List

This section contains a list of the mechanical and/or electrical components that are replaceable for the adjustment/verification fixture. Use this list to identify and order replacement parts. The following table describes each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Manufacturers Cross Index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105–3608
0KB01	STAUFFER SUPPLY CO	810 SE SHERMAN	PORTLAND, OR 97214–4657
13103	THERMALLOY INC	2021 W. VALLEY VIEW LN PO BOX 810839	DALLAS, TX 75381–5381
22526	BERG ELECTRONICS INC	825 OLD TRAIL ROAD	ETTERS, PA 17319
50434	HEWLETT PACKARD	370 W TRIMBLE ROAD	SAN JOSE, CA 95131–1008
53387	3M COMPANY	ELECTRONICS PRODUCTS DIV 3M AUSTIN CENTER	AUSTIN, TX 78769–2963
55285	BERGQUIST COMPANY INC., THE	5300 EDINA INDUSTRIAL BLVD	MINNEAPOLIS, MN 55435–3707
55322	SAMTEC INC	810 PROGRESS BLVD PO BOX 1147	NEW ALBANY, IN 47150
60381	PRECISION INTERCONNECT CORP.	16640 SW 72ND AVE	PORTLAND, OR 97224
75915	LITTELFUSE INC	800 E NORTHWEST HWY	DES PLAINES, IL 60016–3049
93907	CAMCAR DIV OF TEXTRON INC	ATTN: ALICIA SANFORD 516 18TH AVE	ROCKFORD, IL 611045181
TK2449	SINGATRON ENTERPRISE CO LTD	13925 MAGNOLIA AVE	CHINO, CA 91710

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					ADJUSTMENT/VERIFICATION FIXTURE		
B–1–1	131–5267–00			1	CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR	00779	104326–4
–2	131–5829–00			6	CONN,SHUNT:JUMPER,FEMALE,STR,1 EA,2MM,4MM H,	00779	382575–3
–3	131–5990–00			1	CONN,HDR:PCB,MALE,STR,1 X 36,0.079 CTR	55322	TMM–136–02–G–2
–4	131–0608–00			5	CONN,TERMINAL:PRESSFIT/PCB,MALE,STR,0.025 SQ,0.248 MLG X 0.137 TAIL,50 GOLD,PHZ BRZ,W/FERRULE	22526	48283–018
–5	131–6024–00			1	CONN,HDR:PCB,MALE,STR,2 X 25,0.079CTR	53387	151250–8422–TY
–6	105–1089–00			2	LATCH ASSY:LATCH HOUSING ASSY,VERTICAL MOUNT,2/PKG,0.48 H X 1.24 L,W/PCB SINGLE CLIP	60381	105–1089–00
–7	131–6134–00			2	CONN,PLUG:SMD,MICTOR,PCB,FEMALE	00779	767004–1
–8	210–0457–00			6	NUT,PL,ASSEM WA:6–32 X 0.312,STL CD PL,W/LOCKWASHER	0KB01	ORDER BY DESCR
–9	348–0048–00			6	FOOT,CAMERA:BLACK VINYL W/6–32 STUD	80009	348–0048–00
–10	210–0586–00			4	NUT,PL,ASSEM WA:4–40 X 0.25,STL CD PL	0KB01	ORDER BY DESCR
–11	671–3599–00			1	CKT BD ASSY:DESKEW TEST FIXTURE (A14)	80009	671–3599–00
–12	150–5009–00			1	DIODE,OPTO:LED,HI–EFFIC RED,626NM,3.4MCD AT 10MA	50434	HLMP–6305–021
–13	159–5009–00			1	FUSE,SMD:1.5A,125V,FAST BLOW,0.1 X 0.1 X 0.24,UL RECOGNIZED,CSA CERTIFIED	75915	45101.5
–14	131–5527–00			1	JACK,POWER DC:PCB,MALE,RTANG,2MM PIN,11MM H(0.433) X 3.5MM(0.137) TAIL,9MM(0.354) W,TIN,W/SWI	TK2449	DJ–005–A
–15	214–2957–00			2	HEAT SINK,SEMIC:TRANSISTOR,TO–220	13103	6072B
–16	210–1178–00			2	WASHER,SHLDR:TRANSISTOR,TO–220,0.2"ODX0.116	13103	7721–7PPS
–17	211–0372–00			4	SCREW,MACHINE:4–40 X 0.312,PNH,STL CD PL,TORX T10	93907	B80–00020–003
–18	342–0355–00			2	INSULATOR,PLATE:TRANSISTOR,SILICONE RUBBER	55285	7403–09FR–51
–19	131–3378–00			2	CONN,RF JACK:BNC,50 OHM,FEMALE,RTANG,PCB/REAR PNL,0.5–28 THD,0.625 H X 0.187 TAIL,W/O MTG FL	00779	227677–1

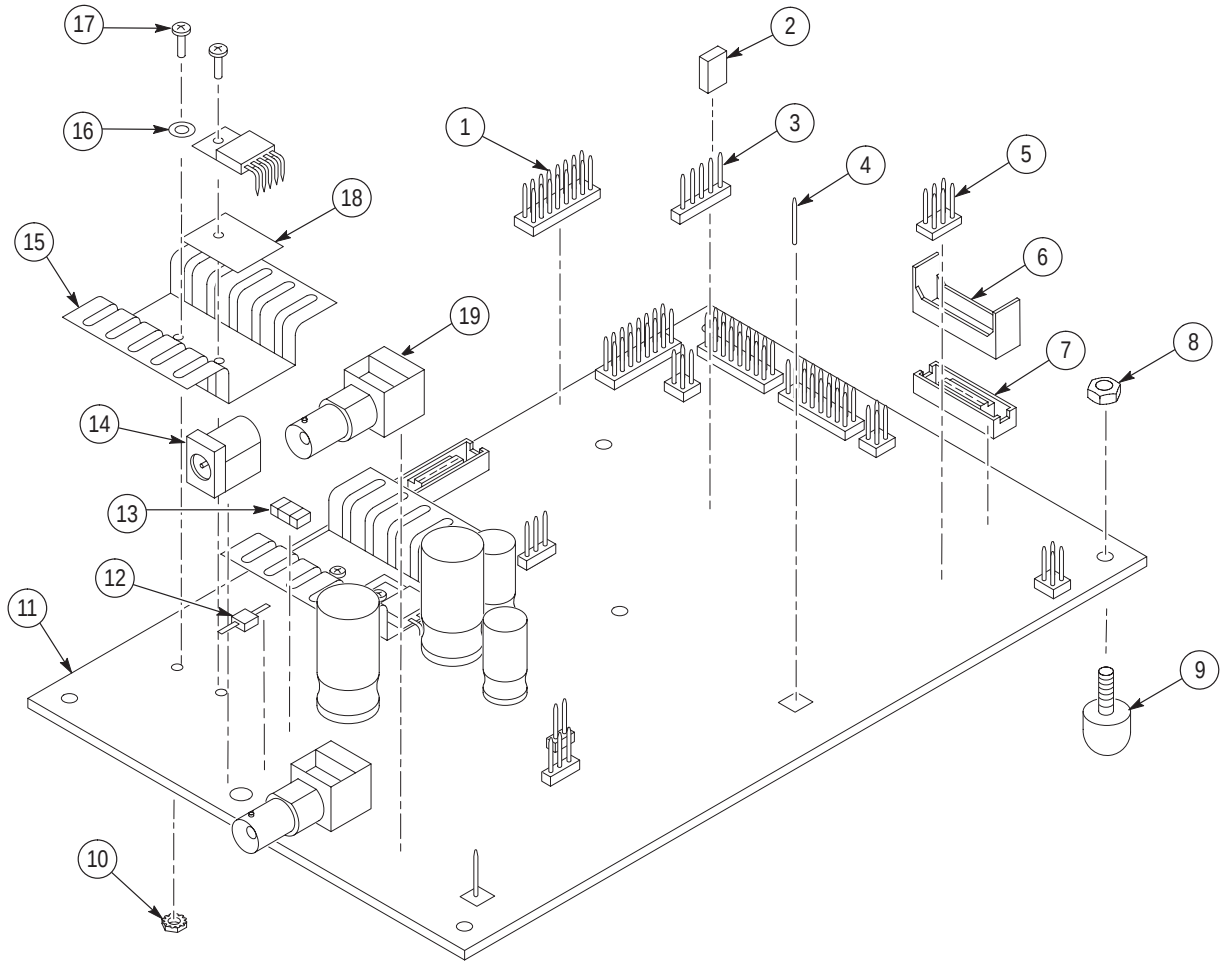

Figure B–1: Adjustment/verification fixture exploded view